Research Journal of Applied Sciences 6 (7-12): 467-472, 2011
ISSN: 1815-932X

Hardware Approach of Fuzzy Inference Based Signature Verification System

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Abstract: This study describe the realization of a signature verification and forgery detection system on Altera FLEX10K FPGA device that allows for efficient hardware implementation. The system follows five steps to perform the signature verification which are data acquisition, preprocessing, comparison process and decision process. Mamdani-type fuzzy inference system is used as the core decision maker for verifying the signature. The timing analysis for the validation, functionality and performance of the model is performed using Aldec Active HDL and the logic synthesis was performed using synplify. The design is modularized and each module is modeled individually using hardware description language VHDL. This is followed by the timing analysis and circuit synthesis for the validation, functionality and performance of the designated circuit which supports the practicality, advantages and effectiveness of the proposed hardware realization for the applications with a maximum clock frequency of 39.80 MHz.

Key words: Signature verification, forgery detection, fuzzy inference, VHDL, FPGA, Malaysia

INTRODUCTION

Electronic signature verification is used to expedite the process of identify users in many areas such as banking, business transaction, industrial application, internet services, shopping and medical to prevent forgery (Elliott and Hunt, 2008; Alonso-Fernandez *et al*., 2007). Most of electronic signature verification schemes require complex functions and a lot of computing power. This is because signature verification requires tools and techniques that recognize signature and represent imprecise, commonsense knowledge about the general appearance of signature (Tan *et al*., 2011).

In this research, researchers are working in a signature verification system that utilizes fuzzy logic and implementing the scheme on hardware. Fuzzy logic, one of several fuzzy set methods, encodes imprecise knowledge and naturally maintains multiple hypotheses that result from the uncertainty and vagueness inherent in real problems. By using the fuzzy approach, recognition capability for solving signature verification problems can be increased. The signature verification system is designed by using Very High Speed Integrated Circuits Hardware Description Language (VHDL). After designing the system in VHDL, the source code is downloaded to Field Programmable Gate Array or FPGA.

FPGA offers a potential alternative to speed up the hardware realization. From the perspective of computer aided design, FPGA comes with the merits of lower cost, higher density and shorter design cycle. It comprises a wide variety of building blocks. Each block consists of programmable look-up table and storage registers where interconnections among these blocks programmed through the hardware description language. This programmability and simplicity of FPGA made it favorable for prototyping digital system (Akter *et al*., 2008; Reaz *et al*., 2003; Alvarez *et al*., 2011).

Literature review shows that several researches had been done in this area. In one of the research, an offline signature verification system receives a two-dimensional image as input from a camera or scanner. The design of a signature verification system requires solutions to five types of problems which are data acquisition, preprocessing, feature extraction, comparison process and performance evaluation (Fang *et al*., 2002). The second research presents approach for the verification of a signature using unique modeling in off-line environment.

Before extraction features, the signature is standardized. This requires a normalization of the scanned signature to the standard size. The signature is thinned to obtain single pixel thick signature which may not be connected. The thinned signature is extracted in terms of distributions of distances and angels with respect to a fixed reference point (Sabourin *et al*., 1997). Another interesting research employs Hidden Markov Models (HMM) for signature verification system. The advantage of modeling signatures with HMM is that it is possible to accept variability in signing and at the same time capture

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the individual features of the signatures. The research utilize HMM Models as a doubly stochastic process governed by an underlying Markov chain with a finite number of states and a set of random functions each of which is associate with one state (Kashi *et al*., 1997; Camino *et al*., 1999).

In this study, the framework of FPGA-based hardware realization of signature verification and forgery detection is proposed. The basic framework utilize the methodology employed by Fang *et al.* (2002) and Sabourin *et al*. (1997) works while employing fuzzy inference system as the core decision maker for verifying the signature. In general, fuzzy inference is the process of formulating the mapping from a given input to an output using fuzzy logic. The mapping then provides a basis from which decisions can be made or patterns discerned. The process of fuzzy inference involves three steps i.e., membership functions, fuzzy logic operators and if-then rules.

There are two types of fuzzy inference systems that can be implemented in the fuzzy logic toolbox: Mamdani-type and Sugeno-type. These two types of inference systems vary somewhat in the way outputs are determined. Based on the study it is found that Mamdani-type is most suitable for this research. It was originally proposed in 1975 by Ebrahim Mamdani as an attempt to control a steam engine and boiler combination by synthesizing a set of linguistic control rules obtained from experienced human operators. Mamdani's effort was based on Lotfi Zadeh, study on fuzzy algorithms for complex systems and decision processes (Fang *et al*., 2002).

In the method, the VHDL is selected as the hardware description language to realize the system. In the computation of method, the problem is first divided into small pieces each can be seen as a submodule in VHDL (Mohd-Yasin *et al*., 2004; Hunter, 1996; Peter, 1996; Reaz *et al*., 2007). Following the software verification of each submodule, the synthesis is then activated that performs the translations of hardware description language code into an equivalent netlist of digital cells. The synthesis helps integrate the design work and provides a higher feasibility to explore a far wider range of architectural alternative (Fawcett, 1994). The method provides a systematic approach for hardware realization, facilitating the rapid prototyping of signature verification and forgery system.

MATERIALS AND METHODS

FPGA realization of signature verification and forgery detection is introduced to implement the hardware based system for this application. The system is capable of verifying signature and prevent forgery. This signature verification system is designed by followed the four steps which are data acquisition, preprocessing, comparison process and decision process. Data acquisition is the method to access to the signature. The signature is scanned and stored as an image, so it can be read by the signature verification system designed. After reading the image, the image will go through the preprocessing part where all the images of signature will be standardized. Next is the comparison process where the signature template will compare with the input signature in terms of mean, standard deviation and correlation. The last step is the decision process where the fuzzy inferencing system is employed using five processes: fuzzification of the input variables, application of the fuzzy operator (AND or OR) in the antecedent, implication from the antecedent to the consequent, aggregation of the consequents across the rules and defuzzification. After this process, the fuzzy inferencing system will result an output according to the inputs.

Data acquisition: In this module, the system will receive signature which is scanned by digital scanner and converted to digital format. Before this, the signature is signed of a clean A4 paper. This step is performed for numerous variation of signatures from the same user. The average of the numerous variations of signatures will be called signature template and the signature to be tested will be called input signature. It is easy to conclude that the more signatures are taken to form signature template, the more accurate result can be gained from the system. For this research, five variations of signatures are considered to form the signature template.

Preprocessing: After data acquisition, the signature will go through a module called preprocessing. The purpose of this module is to standardise the size and format of each signature. This step is performed for each of the five signatures and the input signature. Each signature will be processed as follows. The signature will be first converted to gray scale. After that the gray scale image is turn to binary by setting the threshold of intensity to be 200. The purpose of doing so is to find the-most-right, the-most-left, the-most-upper and the-most-lower point of the signature. By doing this, all the gray scale image can be crop to the size one pixel more than the point found. Then, the gray scale image is resized to the size wanted. After resize, the gray scale image is turn to binary image for better view on the image. Again, the threshold of intensity is set to 200. Then, the image is dilated 3 times compared

to the original image. The dilation is only applicable to the signatures which will form the signature template but not the input signature.

Comparison process: The process followed preprocessing is the comparison module. Before entering comparison module, the system will add the five signatures which are the images after preprocessing. After that the average is taken and this will form signature template. In the comparison process, the input signature will be compared with the signature template. The first image is the sum of five signatures whereas the second image is the signature template. This signature template can be taken to compare with different input signature. The mean, standard deviation and correlation of the difference of signature template and input signature are determined. The three values will be the input of the fuzzy inferencing system. Next, the fuzzy inferencing system will evaluate the input and results an output value.

Decision process employing fuzzy inference: After comparing the input signature with the signature template, the fuzzy inferencing system is activated by the three inputs from the comparison. The system is built of four major functions which are correlation, fuzzy and two Wait_Signals. Each function performs different task. The correlation actually contains a block of components. It was designed to perform the comparison process which compares the input signature and signature template and produces an output value in STD_LOGIC_VECTOR of thirty two bits. In this comparison process only correlation is considered but not mean or standard deviation. The design of correlation block follows the modification of the mathematical equation of correlation. Equation 1 below shows the original correlation:

$$r = \frac{\sum_m \sum_n (A_{mn} - \bar{A})(B_{mn} - \bar{B})}{\sqrt{\left[\sum_m \sum_n (A_{mn} - \bar{A})^2\right]\left[\sum_m \sum_n (B_{mn} - \bar{B})^2\right]}} \quad (1)$$

Where:

$\bar{A}$ = Mean (A)

$\bar{B}$ = Mean (B)

This equation is complex block of components with most of the components perform mathematicaly. However, in this research, the inverse of correlation was considered rather than correlation because it is a hard work to handle floating point in VHDL. Moreover, VHDL cannot handle multi-dimensional arrays and square roots. Therefore, the equation had been modified for the VHDL implementation as shown in Eq. 2:

$$R^2 = \left(\frac{1}{r}\right)^2 = \frac{\left[\sum_i (A_i - \bar{A})^2\right]\left[\sum_i (B_i - \bar{B})^2\right]}{\left[\sum_i (A_i - \bar{A})(B_i - \bar{B})\right]^2} \quad (2)$$

The correlation function is enabled by the first Wait_Signal after the enable of the system is activated. Then, the comparison process will start. After finishing the task, the Correlation will send a signal to second Wait_Signal. The second Wait_Signal works as the first Wait_Signal which is activated by a signal and send out the other signal to enable other block. The purpose of doing so is to make sure the fuzzy inference system works after correlation function finished its task. The fuzzy inference system works in a similar method as the correlation function. The Mamdani-type logic toolbox is employed for this study. Then, an output is resulted whether the input signature matched or unmatched with the stored signature.

Number format design: Since, finite storage devices also referred to as sequential elements are being used in the chip, the internal signals must have a numbering format. In this study, number-scaling method is used to reduce the complexity and to facilitate synthesis process. This method multiplies integer type of VHDL with 1024 or 1024^2 depending on the number of multiplication and later divides the number with the same constant in order to get back its initial value.

RESULTS AND DISCUSSION

The system was coded in IEEE-compliant VHDL and compiled and simulated using the Aldec Active-HDL Version 3.5 suite. This provides an opportunity to detect and correct errors early in the design process (Mohd-Yasin *et al*., 2004; Hunter, 1996; Peter, 1996; Reaz *et al*., 2007). All modules were designed and tested in isolation before being incorporated into the higher levels of the design. The final step which is the synthesis is done using synplify. The results are generated using waveform editor. The average percentage of accuracy achieved is 87.38%. In this study two simulations are shown in two sections below using the 72 bit input binary data. The clock signal and outputs are given in the timing diagram.

Simulation on correlation module: The correlation is the block which executes the comparison process. This block compares the input signature with the signature template and results a value which is assigned to data_out. Once this block finish task, one signal is send to activate the Fuzzy indirectly. The simulation was done on matched

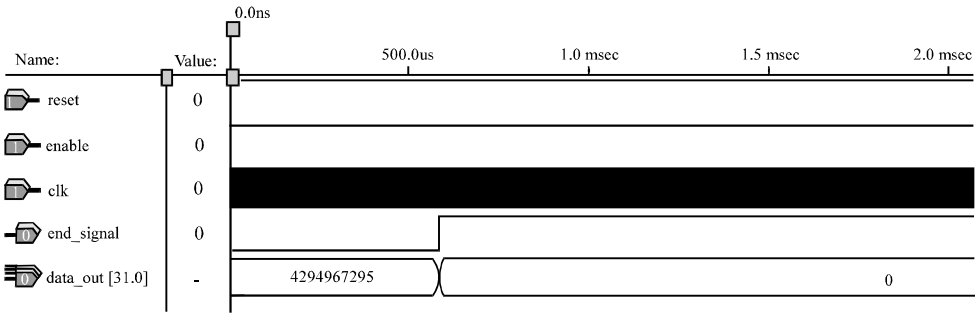

Fig. 1: Correlation simulation for matched signature

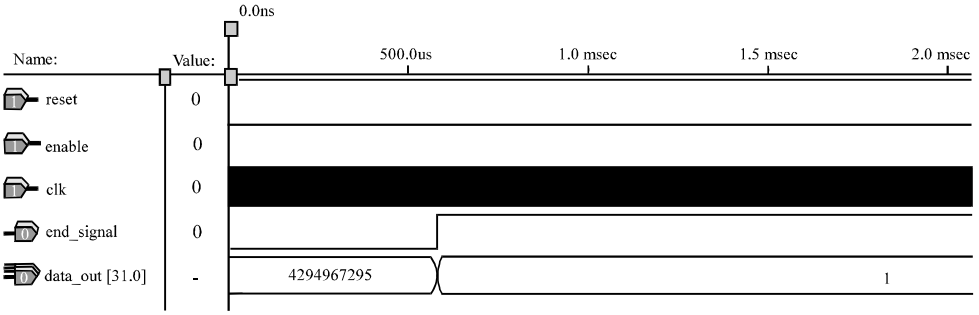

Fig. 2: Correlation simulation for forged signature

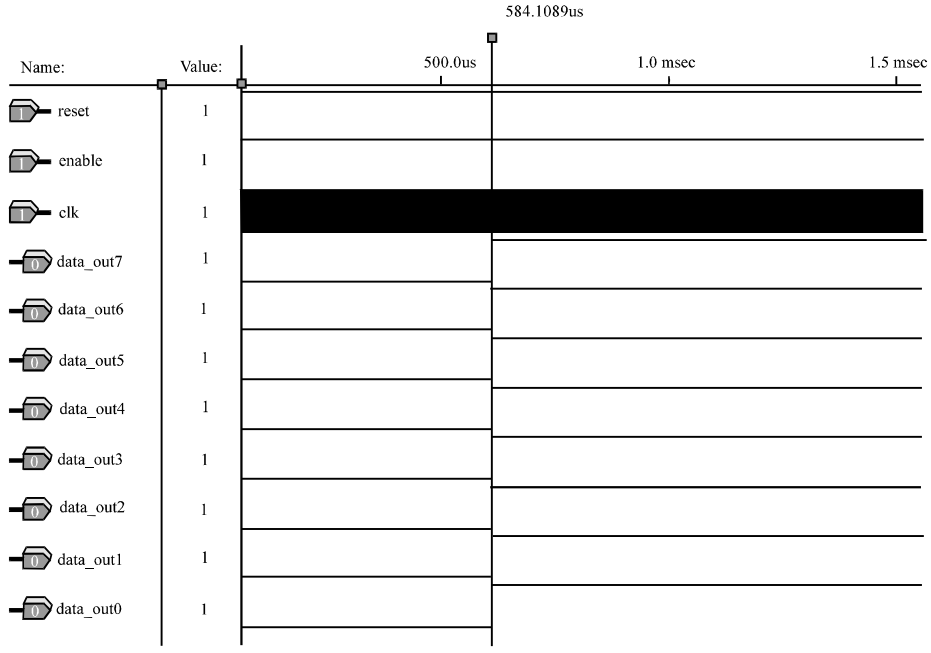

Fig. 3: Signature verification system timing diagram for matched signature

signature and forged signature. Figure 1 shows the result for the matched signature and Fig. 2 shows the result for forged signature. It can easily verified that the correlation function works as expected.

Simulation on signature verification system: The signature verification system designed has three inputs and one eight bits of STD_LOGIC_VECTOR output. The reset was set to 1 at 100.0ns and the enable was set to 1

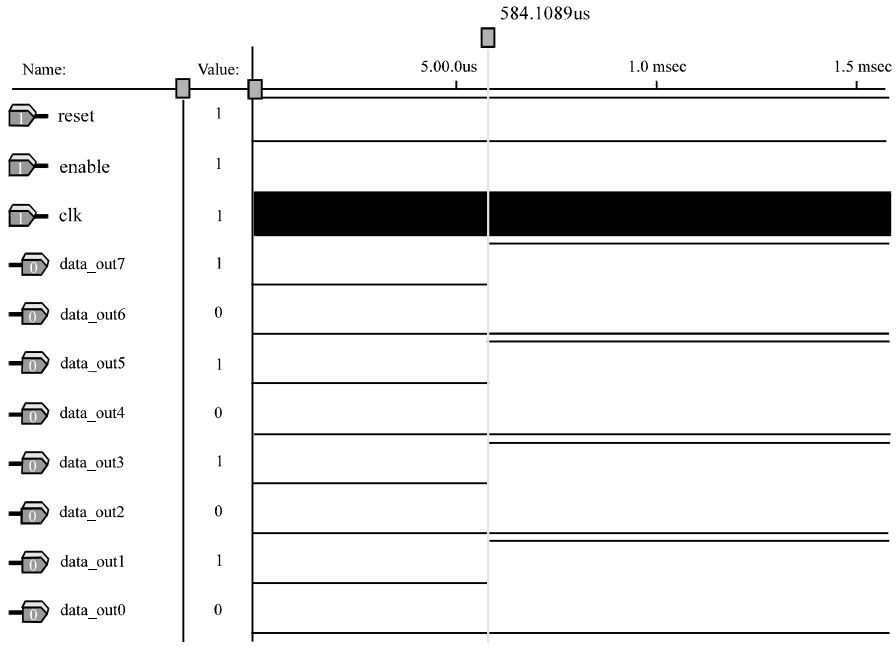

Fig. 4: Signature verification system timing diagram for forged signature

Table 1: The usage of logic resources in EPF10K10LC84

Logic resources	Values
LCs used	366 LCs out of 576 (63.54%)
Number of nets	444
Number of inputs	1843
I/O cells	66
Cells in logic mode	323
Cells in cascade mode	43

at 300.0ns. The frequency of clk used for the simulation is 3.33 MHz. Both matched and forged signature input had been tested. The outputs from Fig. 3 and 4 show the correct results at 584.1089us for one test case.

Synthesis: In regard to the designated hardware realization. The VHDL code is synthesized by considering Altera FLEX10K: EPF10K10LC84 FPGA chip on LC84 package. The physical hardware layout is generated using the synthesis tool Synplify Version 7.0. The FLEX 10K family provides the density, speed and features to integrate entire systems including multiple 32 bit buses into a single chip. A comparatively low critical path frequency was achieved which was 39.80 MHz. The design took a minimum resource i.e., 366 logic cells which is 63.54% of the device EPF10K10LC84. Table 1 shows a details report of the usage of resources.

CONCLUSION

This research has been dedicated to design and implement a simple yet efficient signature verification system employing FPGA. The system employs fuzzy inference system in the decision. The modules were successfully compiled and simulated. The hardware implementation demonstrated complete, correct functionality and met all the initial system requirements. Using IEEE floating point-numbering format would enhance the accuracy of algorithm. Currently, researchers are conducting further research that considers the floating point numbering format and the further reductions in the hardware complexity to achieve better performance.

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