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LNA and Mixer for Broadband Digital Video Broadcasting (DVB) Application Using CMOS Process

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Abstract: In this study, the broadband Low Noise Amplifier (LNA)/mixer for Digital Video Broadcasting-Satellite (DVB-S2) receiver tuner integrated circuit-fabricated using 0.18 μm Complementary Metal Oxide Semiconductor (CMOS) process is proposed by applying a positive feedback to LNA and adding a Single-ended Differential Converter (SDC) to mixer. And 2 attenuators are used to obtain a good noise performance and high linearity property. The designed CMOS LNA/mixer have achieved the control of gain with 3 dB step, input second order intercept point (IIP2) of 1.37 dBm and input third order intercept point (IIP3) of -3.6 dBm at high gain low frequency mode. Moreover, a noise figure of 6.4 dB has been achieved at the frequency range from 950-2150 MHz. The LNA circuit consumes a total current of 25 mA together with the supply voltage of 1.8 V and the chip area of LNA and mixer are 0.8×0.53 and 0.8×0.6 mm, respectively.

Key words: LNA, mixer, DVB-S2, CMOS, broadband

INTRODUCTION

DVB-S2 is a digital television broadcast standard that has been designed as a successor for the popular DVB-S system (ETSI, 2009). It was developed in 2003 by the DVB Project (Tsividis, 1998). The standard is based on and improves upon DVB-S and the Digital Satellite News Gathering system (DSNG), used by mobile units for sending sounds and images from remote locations world-wide back to their home television stations (ETSI, 2005). DVB-S2 achieves a significantly better performance than its predecessors-mainly allowing for an increase of available transmission capacity over same satellite transponder bandwidth. The measured DVB-S2 performance gain over DVB-S is around 30% at the same satellite transponder bandwidth and emitted signal power (Morello and Mignone, 2004). The main targets of standard revision are to guarantee a much higher transmission capacity and to improve service capability through the enhanced link margin and the realization of a new service requirement for broadband broadcasting like HDTV, interactive services, including internet access, digital TV contribution and news gathering, etc. (DVB Project Office, 2013). However, there is a limitation to bandwidth in the DVB-S1 system, such as the Ka-band satellite broadcasting and the Carrier-to-Noise (C/N) ratio has also been estimated to be about 0.5 dB sec^{-1} during heavy rain fades in the first version of DVB-S (Larson, 1996; Morello and Mignone, 2006).

As for this DVB-S2, the LNA/mixer is designed and fabricated using the dominant integrated-circuit manufacturing technology-Complementary Metal Oxide Semiconductor (CMOS). The main advantage of CMOS over N-Mental-Oxide-Semiconductor (NMOS) and bipolar technology is the much smaller power dissipation. Unlike, NMOS or bipolar circuits, a CMOS circuit has almost no static power dissipation. Power is only dissipated unless the circuit actually switches. This allows integrating many more CMOS gates on an IC than in NMOS or bipolar technology, resulting in much better performance (Westergaard, 2001). By using this technology, the LNA/mixer can achieve a low-dissipation property and compact size. It can be predicted that CMOS will remain, as a mainstream in the foreseeable future technologies and the reduction of CMOS device dimensions still has a long way to go. It is realistic to expect device performance to be increased, as efforts continue contributing in technology scaling for the next decade (Shin *et al*., 2006).

The block diagram of the proposed LNA/mixer is shown in Fig. 1. In this study, by applying a positive feedback to LNA and adding a SDC to mixer, a broadband 950-2150 MHz can be obtained for the application of DVB-S2 system. In addition, a 12 dB attenuator and 3·6·9 attenuator are applied in front of and behind the LNA, respectively in order to obtain a good noise performance and high linearity property.

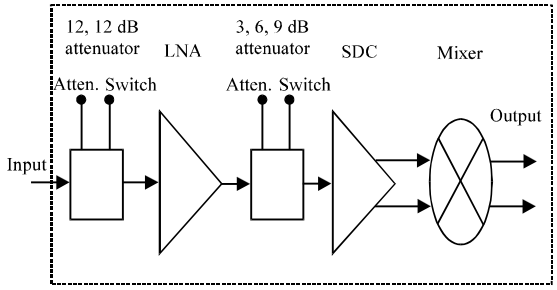

Fig. 1: Block diagram of LNA/mixer

Circuit design techniques: Attenuator is used to control the gain mode through the power variation of input signal. To accommodate large signals and strong blockers, a gain step is necessary for the LNA to realize the linearity requirements of the mixer. The proposed attenuators are designed in pi (π) type. The gain is controlled with 3 dB step by using 12 dB and 3·6·9 dB attenuators.

Figure 2 shows the 12 dB attenuator. By cascading two 12 dB attenuators, a total 24 dB attenuation is obtained. The cascaded attenuators operate through two paths. One is through path and the other is attenuation path, the 2 paths can separate the gain into 3 mode which are high gain mode, medium gain mode and low gain mode. When the channel of Q_1 is on and those of Q_2 and Q_3 are off, so that most signals pass through the channel of Q_1, called as through pass. At this condition, the channel resistance and parasitic capacitance of Q_1 can attenuate the signal. For this reason, the size of Q_1 is considered to be large. But if the size of Q_1 is too large, the parasitic capacitance also increases. When the channel of Q_1 is off and those of Q_2 and Q_3 are on, so that signals pass through the pi (π) attenuator, called as attenuation path. Also, the channel resistance and the parasitic capacitance of Q_{1-3} can affect the amount of attenuation and frequency characteristic.

In general, 2 cascade 12 dB attenuators can form a 12, 24 dB attenuation mode. Figure 3 shows the 3, 6, 9 dB attenuator. The 3·6·9 dB attenuator controls gain with 3 dB step at each gain mode which is separated by 12 dB attenuator. And the position of 3·6·9 dB attenuator is next to LNA, so that it does not affect noise figure strongly. In Fig. 3, each transistor and resister of 3, 6 and 9 dB attenuator is connected in parallel. When the channel of Q_1 is on and those of the others are off, so that most signals pass through the channel of Q_1, call as through path or through mode. When the channel of Q_1 is off and those of Q_{2-4} are on, so that signals pass through the pi (π) attenuator. Therefore, it can be conclude that if the channel of Q_{2-4} or Q_{5-7} or Q_{8-10} are on, signals pass

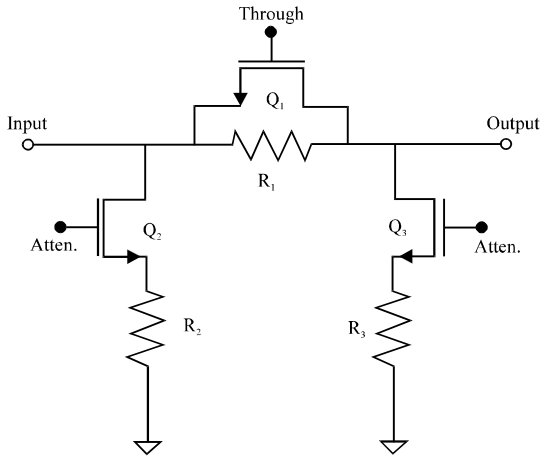

Fig. 2: The 12 dB attenuator

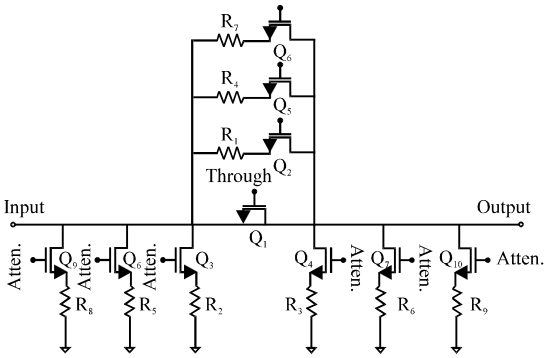

Fig. 3: The 3, 6, 9 dB attenuator

through 3 dB or 6 or 9 dB attenuator, respectively called as 3·6·9 dB attenuation mode. The channel of Q_1 is always off at attenuation mode.

The circuit in Fig. 3 can form two modes: Through mode and 3·6·9 dB attenuation mode. Figure 4 shows S21 at through mode and 3, 6, 9 dB attenuation mode. Attenuation quantity of simulation and measurement in the frequency range of from 950-2150 MHz is roughly 2.6-3.1 dB. Also Fig. 5, shows the simulation and measurement results of S21 at 12 and 24 dB attenuation mode are in good agreement. The flatness of total gain at each attenuation mode is under 3 dB. Figure 6 and 7 show the simulation and measurement results of S21 controlled with 3 dB step at each gain mode.

LNA: In designing the broadband LNA, it is necessary for the LNA to provide gain to weak signals from the antenna and the least possible contribution to the noise, so that the Signal to Noise Ratio (SNR) is not lowered by the circuit. Another feature of the LNA is the ability to handle large signals without distortion. The design of a LNA

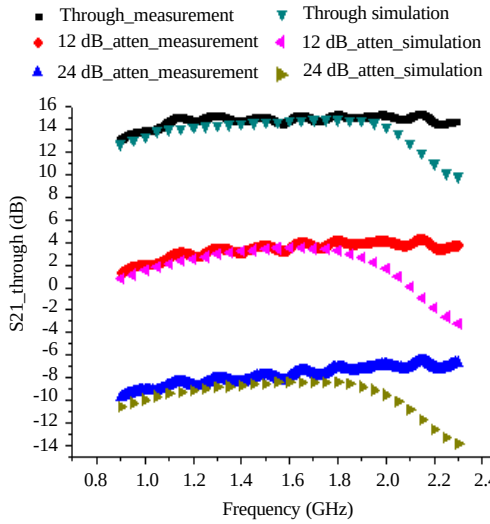

Fig. 4: S21 at 3, 6, 9 dB attenuation mode

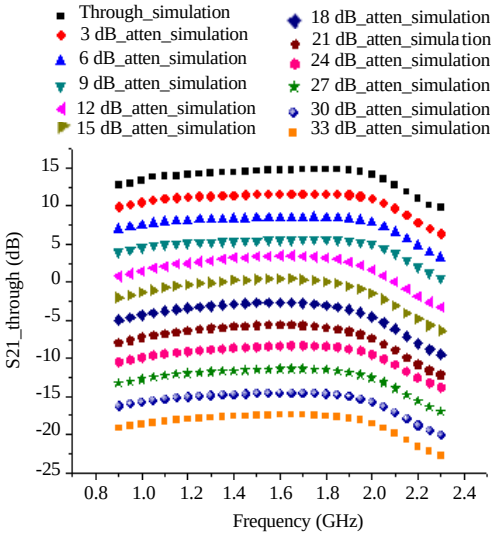

Fig. 6: Simulation result of total S21 with 3 dB step

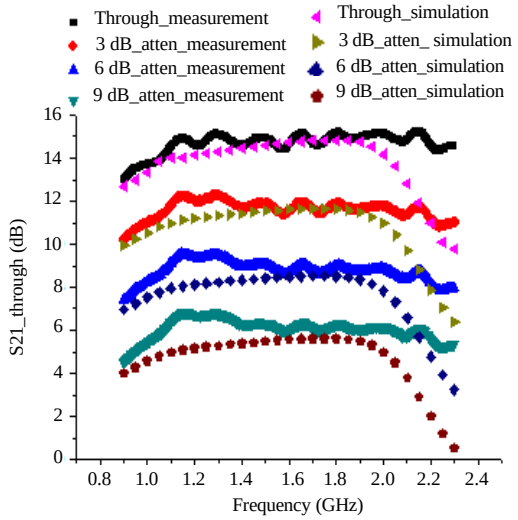

Fig. 5: S21 at 12 and 24 dB attenuation mode

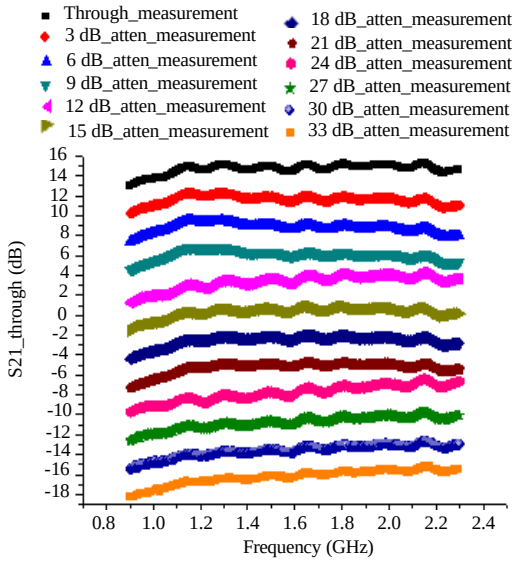

Fig. 7: Measurement result of total S21 with 3 dB step

involves numerous tradeoffs. The amplifier must have sufficient gain to overcome mixer noise problem but not so much to cause mixer overload at the meantime. Good noise characteristics are preferred while achieving desired input and output matching. The matching networks at the input and output of the LNA often need a compromise between optimum gain matching and optimum noise figure matching. Selecting a technology and package involves tradeoffs of cost and level of integration.

LNA occupies a significant percentage of the total die area in wireless front-end of DVB-S2 today. It is because the performance of the LNA is dependent on the Q-value of the on-chip inductors. The design of these circuits usually requires a larger die size, a higher number of simulation and verification iterations. Figure 8 shows

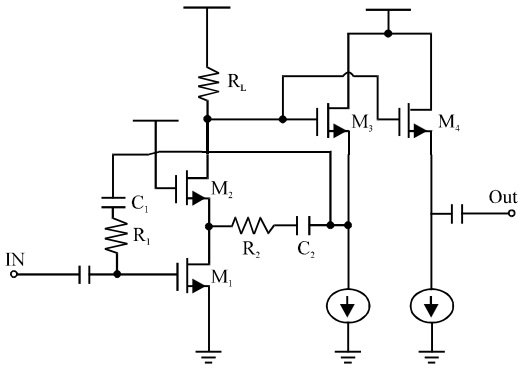

Fig. 8: Inductorless LNA using a positive feedback

an inductorless broad-band LNA using a positive feedback. This circuit can significantly reduce the cost of the wireless front-end implementation of DVB-S2. Generally, 75 Ohms termination is used for minimum distortion characteristic in DVB-S2 receiver. Therefore, the input termination of LNA core is 75 Ohms and the output termination is 50 Ohms due to the input impedance of Single-ended Differential Converter (SDC). This LNA must feature 75 Ohms input matching, a good gain flatness and a low noise figure over the entire Bandwidth (Kim *et al*., 2003).

The common-source cascaded amplifier, the most commonly used circuit topology for LNA is used to reduce the Miller effect of the input device M1 and to achieve improved reverse isolation due to high output impedance at the drain of the cascaded device M2. Supply voltage is chosen at 2.7 V and supplied by Low Drop Output (LDO). LDO transforms the supply voltage from 3.3 V into 2.7 V. Open loop gain is roughly gm 1×RL. The parasitic capacitance CL and RL create a pole and limit the bandwidth of amplifier. A positive feedback capacitance C2 compensates for parasitic capacitance CL and improves the bandwidth. The input impedance at moderate frequencies is

$$R_{in} \cong \frac{R_F}{1+A_V} \cong \frac{R_F}{A_V}$$

Where, AV is the voltage gain. Proper choice of R_F provides input matching. However, even with the positive feedback capacitance C_2, the amplifier still has limited bandwidth. Typically, only R_F is included and input matching degrades at higher frequency due to gain roll-off and input capacitance. And matching can be enhanced with off-chip input inductance, such as a bond wire and properly sizing R_L, M_3 and I_3. The input impedance of M_3 is inductive, given by:

$$L_{EQ} \cong C_{gs3}\frac{R_L}{g_{m3}} = \frac{R_L}{2\pi f_{t3}}$$

LEQ can be chosen to resonate with this parasitic capacitance. A separate source follower M4 provides better reverse isolation and the required capability to drive single-ended differential converter. The output current of M4 will typically be sent to single-ended differential converter through 3·6·9 dB attenuator.

The simulation result of S11 is less than 6.8 dB and the measurement result is below 7.7 dB in Fig. 9. The simulation and measurement result of S21 at high gain mode is shown in Fig. 10. S21 is 12-14.8 dB in simulation and 13.5-15.2 dB in measurement. Figure 11 shows the

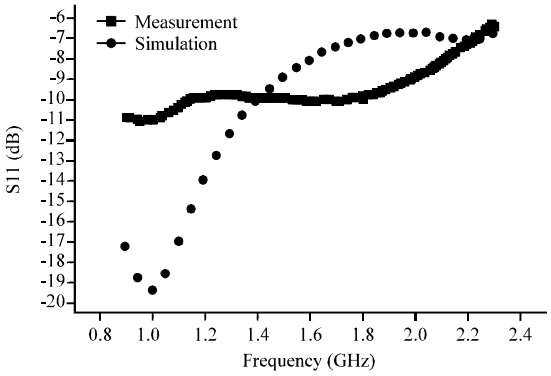

Fig. 9: S11 at high gain mode

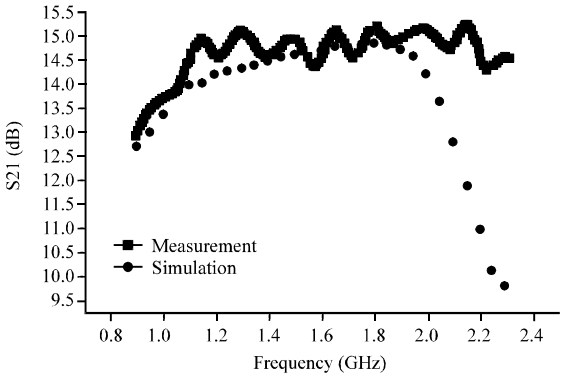

Fig. 10: S21 at high gain mode

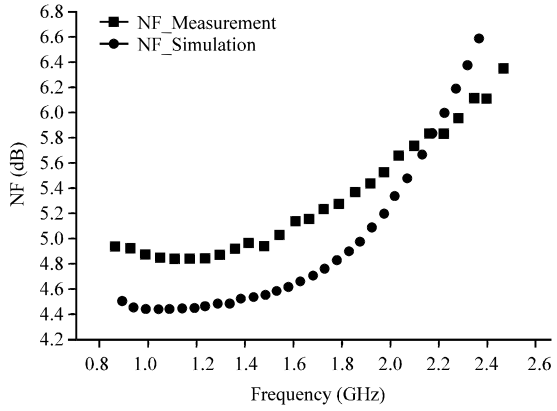

Fig. 11: Noise fighure at high gain mode

simulation and measurement results of noise figure. Noise figure is under 5.6 dB in simulation and under 5.7 dB in measurement. The noise measurement has been performed by using a noise figure meter in the shield room.

Mixer: Figure 12 shows the SDC and quadrature down-conversion mixer. SDC converts the single output signal of LNA to differential output signals and acts as a

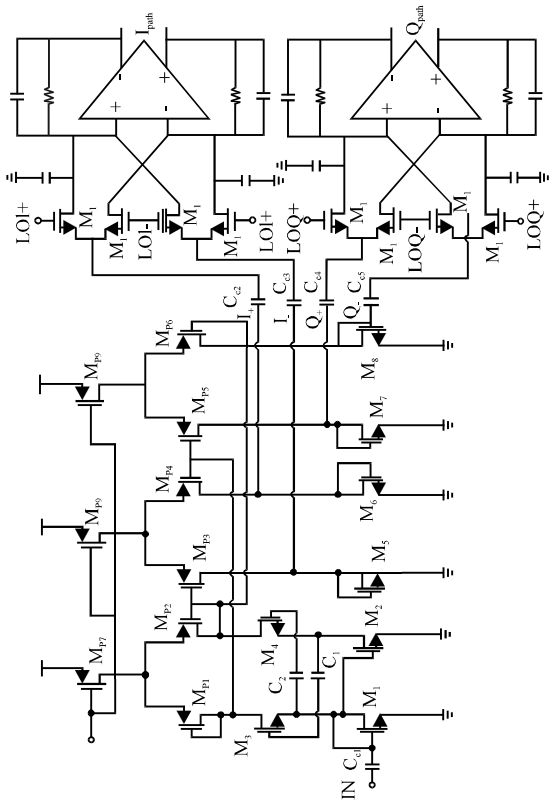

Fig. 12: SDC and passive mixer

transconductor with an equivalent current gain (g). By applying current mirror structure, SDC has a good broadband characteristic and high linearity to endure strong analog/digital adjacent channel interference signals. The Positive channel Metal Oxide Semiconductor (PMOS) transistors (MP_1 and MP_4, MP_5, MP_2 and MP_3, MP_6) compose a current mirror. The current mirror can amplify ac/dc current as the size ratio of $(WP_4/LP_4)/(WP_1/LP_1)$ and $(WP_2/LP_2)/(WP_3/LP_3)$. But, the size ratio of this circuit are 1 and 1. Because if amplified signal through LNA is re-amplified by SDC, this front-end can not get high linearity.

Each signal comes from LNA is converted to differential signals by M_1 and M_2. The sizes of M_1 and M_2, M_3 and M_4 are decided by minimizing amplitude mismatch between differential signals. The impedance of M_1, M_3 at node A and M_2, M_4 at node B should be equivalent to get signals with equal amplitude at drain of M_1, M_2 and the value is about 1 g^{-1}. The resistance of diode connected load is relatively small ($\approx 1\ g^{-1}$) which enables the current mirror circuit to have a flat gain response in a wideband. Current sources (MP_{7-9}) improve the amplitude and phase mismatch of differential current signals are decreased by making 2 diode-connected loads differential pair. However, it can make linearity poor by not having

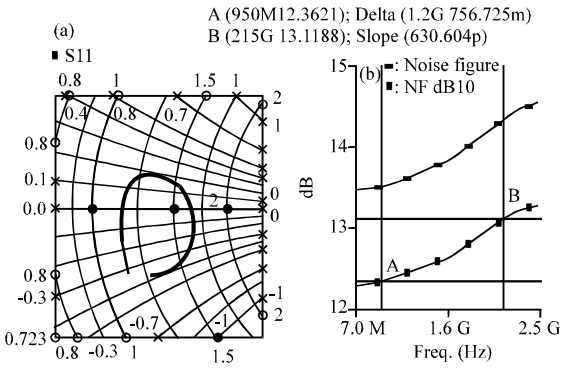

Fig. 13: S11 and noise figure: a) S-parameter response; b) Noise response

enough headroom. For this reason, the current mirror load and current source use 3.3 V PMOS in place of 1.8 V PMOS and 2.7 V VDD supplied by external voltage regulator. And in order to further decrease the phase mismatch, the cross-coupling capacitors C_1 and C_2 are added to common gate amplifier and used 1 pF Metal-Insulator-Metal (MIM) capacitors. The 2 current mirror stages are added to drive the current to the quadrature passive mixer technical brief SWRA030 (Loy, 1999).

Down-conversion is performed by 2 (I_{path} and Q_{path}) double balanced passive mixers, each consists of 4 MOS transistors operating in the triode region, as shown in Fig. 12. The LO signals are ac coupled to the mixers which can improve I-Q balance and allow to optimize the DC bias of the switching pairs for noise and linearity. Choosing a static overdrive voltage close to zero drastically reduces the flicker noise contribution while giving excellent linearity. To have high linearity, low noise and reduced LO radiation, the mixer should have a very low impedance load. On the other hand, the conversion gain is proportional to the feedback resistance. Loading the mixer with the virtual grounds of a fully differential operational amplifier with two 500 ohms resistors connected in feedback achieves both objectives. The opamp noise must be minimized for 2 reasons. First, the connection of both I_{path} and Q_{path} mixers to the LNA output causes a transconductance loss of about 3 dB. Second, there is an equivalent resistor across the 2 virtual ground nodes produced by the switching of the parasitic capacitors at the LNA side that amplify the opamp noise (Razavi, 1998).

Figure 13 shows S11 and noise figure simulation results of SDC. S11 of SDC is (1/2 g)+α by common gate structure, over 60 Ohms in the frequency range of 950-2150 MHz. And noise figure is 12.3-13.1 dB.

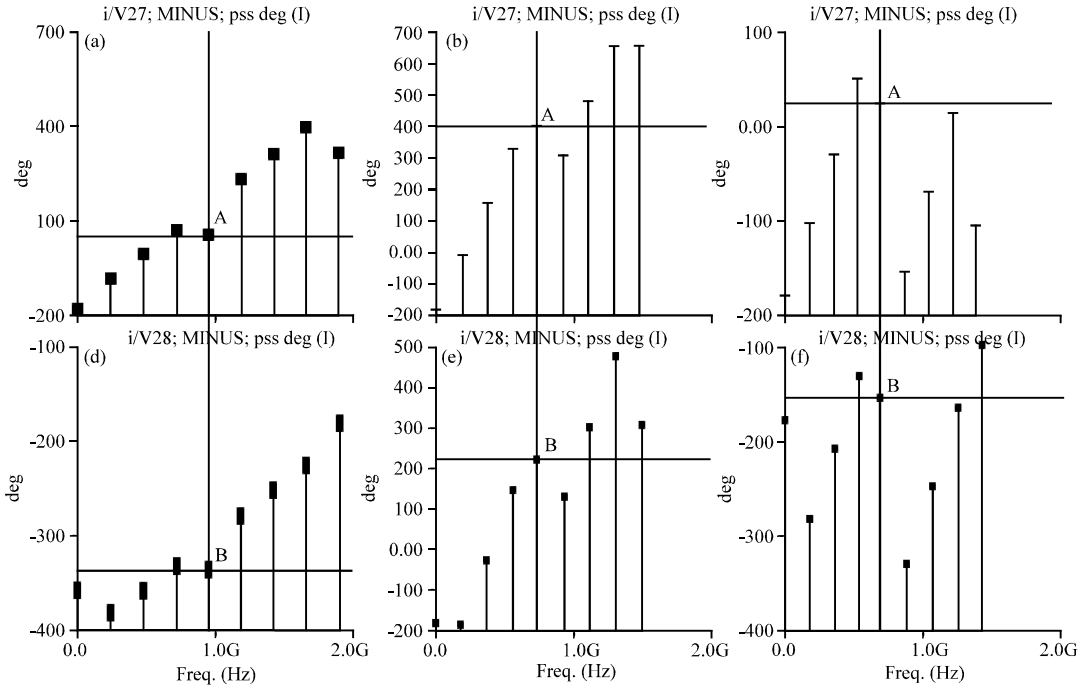

Fig. 14: Phase mismatch of SDC; periodic steady state response

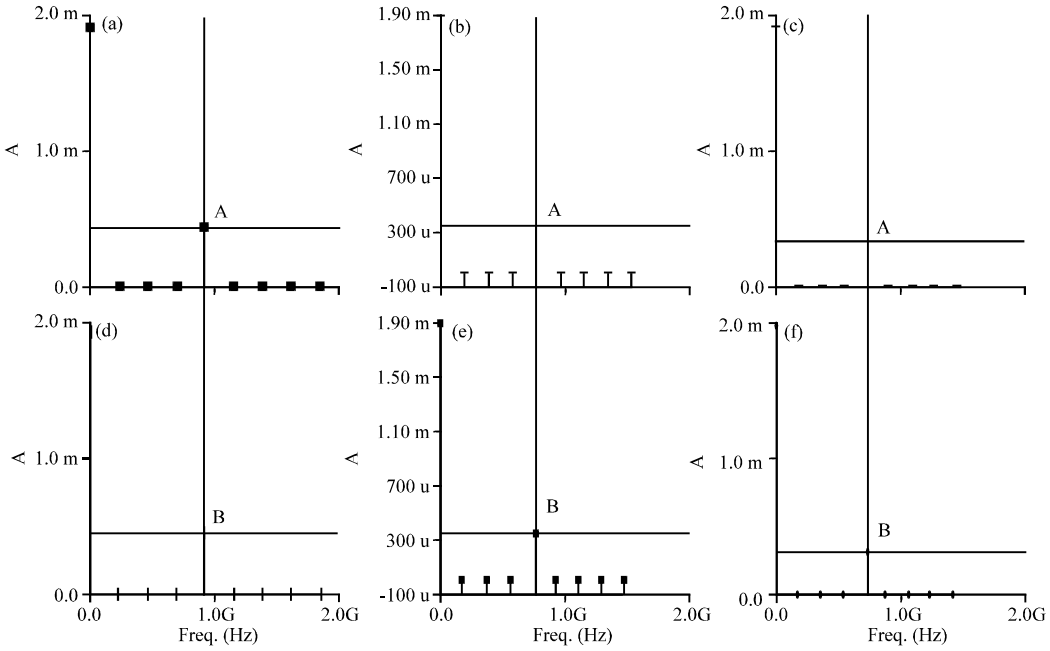

Fig. 15: Amplitude mismatch of SDC

Figure 14 shows phase mismatch of SDC. Each phase mismatch at 950, 1550 and 2150 MHz is 179.1, 178.7 and 179°. Each amplitude mismatch at 950, 1550 and 2150 MHz is 1.45, 10.8 and 29.6 μA, 0.3-8% in Fig. 15.

The simulation results of IIP3 and IIP2 are shown in Fig. 16. IIP2 and IIP3 of SDC are 38.1 and 11.8 dBm.

Finally, a usage of grounding is also very important to design RF circuit. In this design, LNA has 4 grounds

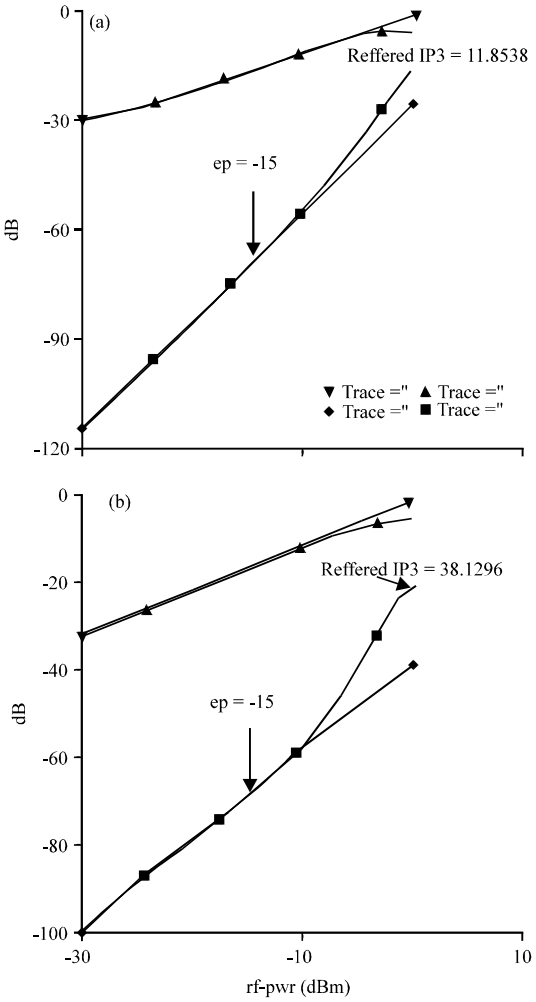

Fig. 16: IIP2 and IIP3 of SDC; periodic AC response: a) Net = (net95/97) 3rd order freq. = 970M; 1st order freq. = 950M; b) Net = (net95/97) 3rd order freq. = 960M; 1st order freq. = 950M

and single-ended differential converter has 2 grounds. About 12 and 3·6·9 dB attenuators has totally 3 ground capacitances.

Simulation and measurement: The simulation is performed by Cadence Spectre RF. A LNA and mixer with SDC are simulated for DVB-S2 receiver Tuner IC application. Total power consumption is 45.9 mW and current consumption is 25.5 mA which is 19.5 mA for LNA and 6 mA for mixer, respectively. The broadband LNA and mixer are fabricated using Taiwan Semiconductor Manufacturing Company (TSMC)'s 0.18 μm Mixed Mode RF 1P6M process. The fabricated Multi-Project Wafer (MPW) chips are packaged by 5×5 mm Quad Flat No-lead Package (QFN).

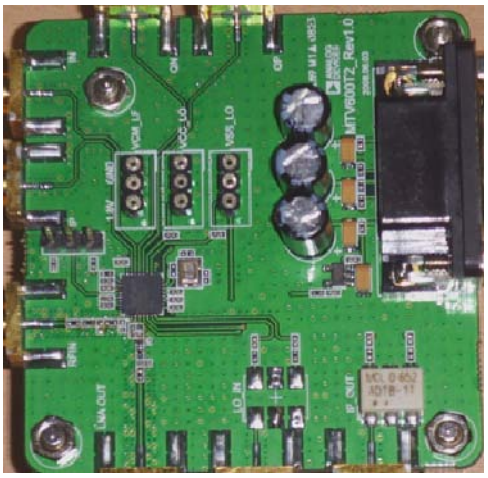

Fig. 17: The photograph of chip on the PCB

Table 1: Summary of measurement results

Parameters	Unit	Measurement
Frequency range	MHz	950-2150
Power consumption	mW	45.9
Noise figure @ high gain mode	dB	5.1-6.4
IIP2 @ high gain low frequency mode	dBm	1.37
IIP3 @ high gain low frequency mode	dBm	-3.6

The packaged chip photo is shown in Fig. 17 and Table 1 shows the summary of the over all measurement performance.

CONCLUSION

The LNA/mixer is proposed to achieve broadband property for DVB-S2 receiver tuner IC application. It has been designed and fabricated in 0.18 μm Mixed Mode RF CMOS process. A positive feedback has been introduced to achieve the broadband characteristic in designing LNA, a SDC has been designed with current mirror structure in designing mixer for the broad-band characteristic and high linearity. By adding 2 attenuators, LNA realizes good NF performance at high gain mode and high linearity characteristic at low gain mode. The total gain is controlled with 3 dB step by 3·6·9 dB attenuator. Moreover, SDC uses cross-coupled capacitor and current source binding differential load for low phase and amplitude mismatch property. There are some discrepancies between simulation and measurement results. The main reason is due to the broad-band impedance matching.

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