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On Ways to Improve Adaptive Adjoint LMS Algorithm Using High Speed Architecture

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Abstract: This study proposes a technique termed Adjoint LMS which provides a simple alternative to the other adaptive algorithms. Here we implement Adjoint LMS algorithm into VLSI using Verilog HDL. This ASIC chip is designed, simulated and synthesized using Xilinx FPGA Virtex 2P (2vp30ff896-6) and the workability of the algorithm is tested for noise cancellation and verified using matlab.

Key words: Adaptivefilters, adjointlms, filtered-XLMS, floorplanning, FPGA

INTRODUCTION

Recent developments in Field-Programmable Gate Arrays (FPGA) technology have changed the traditional method of implementations (Lok-Kee and Roger, 2005). Today, the computational task for the signal processors has been increased dramatically with added fuctions to perform the more intensive tasks. FPGA provide good combinational high-speed implementation features with flexibility. FPGA has grown over the past decade to the point where there is now an assortment of adaptive algorithms which can be implemented on a single FPGA device.

Adaptive filtering has been a key enabling ingredient in many current as well as newly emerging communication technologies (Bernard and Samuel, 2002). Today, adaptive filtering techniques are used to overcome channel limitations and mitigate echoes in high speed digital subscriber loops and gigabyte networks (Haykins, 1996). The need for Adjoint LMS algorithm is to get fastest convergence algorithm, error reduction and Signal to Noise Ratio (SNR) compared to other LMS algorithms. In Adjoint LMS, the error (rather than the input) is filtered through an adjoint filter of the error channel. Performance regarding convergence and misadjustment are equivalent. Compared to all LMS algorithms, Adjoint LMS algorithm is the best one. Here two secondary filters in the input side and one in feed back side are used. By this, error is reduced (Johnson and Larimore, 1997). Adjoint LMS algorithm has been proposed in the literature (Eric, 1996). Several Filtered X-LMS algorithm' have been proposed in the literature (Rupp, 1995, 1997). However, the real time implementation of Adjoint LMS algorithm has largely remain unexplored.Recently, a computationally-efficient pipelined LMS algorithm using Virtex FPGA was proposed in Lok-Kee (2005).

In this study, we present a VLSI architecture for the Adjoint LMS task. The architecture employs two-input, one-output Adjoint LMS chip with self contained control logic. The system can be operated at a frequency of 27 MHz has been designed for fabrication in 0.6 μm technology using Xilinx FPGA Virtex 2P (2vp 30ff 896-6) tools.

ALGORITHM

As shown in Fig. 1, the input vector x(n) through the adaptive filter coefficients vector w(n-1) produces the filter output vector y(n). Filter's y(n) through the secondary path filter,s produces the secondary actuator response at the sensor ys(n). The error is formed by adding the signal rather than subtracting them to be compatible with real world sensors such as microphones and accelerometers. The evaluated error signal is defined by e(n) = d(n) + ys(n). The mirrored error vector e(n) through the estimate of the secondary path se produces

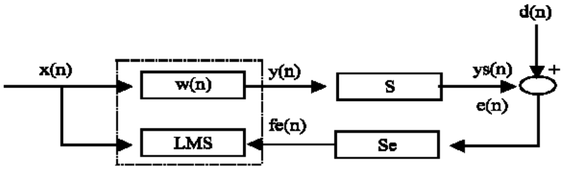

Fig. 1: Block diagram of adjoint LMS

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the filter-error signal fe(n). x(n) and fe(n) is used to calculate the normalized gradient vector and uses this to update the adaptive filter coefficients w(n) and supports both real and complex signals (Emmanuel and Barrie, 2002).

The wiener solution to the above problem is given by $w(\omega) = s(\omega)^{-1}\ p(\omega)$ where $w(\omega)$ is the controller response at frequency ω. $s(\omega)$ is the response of the secondary path and $p(\omega)$ is the response of the primary of the secondary path. At the same frequency the adaptive controller will asymptotically approach this wiener solutions provided that $s(\omega)$ is a minimum phase functions (does not have zeros outside the unit circle) and the controller length is large enough to accommodate the above convolution. If $s(\omega)$ is not minimum phase functions, the adaptive controller will approach the causal part of the solutions. If the controller is too short, the solutions will be truncated. In both cases the noise reduction at the sensor is decreased.

RESULTS AND DISCUSSION

The application of Adaptive filters for active noise control using Adjoint LMS algorithm is implemented using matlab for a random input and it is plotted in Fig. 2, for various adaptation step sizes and it clearly shows that the algorithm converges for the step size of 0.01 to 0.10, here the convergence of error is very high when compared to Filtered-XLMS adaptive algorithm and stability is maintained.

For different step sizes the variance, mean, mean square error and the signal to noise ratio for the Adjoint LMS algorithm is tabulated in Table 1 and plotted in Fig. 3. It picturizes the mean, variance, MSE and SNR values for various step sizes and differentiates clearly the convergence of the algorithm for various step sizes, giving the different values.

User-programmable gate arrays, called Field-Programmable Gate Arrays (FPGAs), have emerged and have changed the way electronic systems are designed and implemented. FPGA chips are prefabricated as arrays of identical programmable logic blocks with routing resources and are configured by the user into the desired circuit functionality. The most popular FPGA architectures use either a Look-Up-Table (LUT) or a multiplexer-configuration as the basic building block. With the growing complexity of the logic circuits that could be packed on an FPGA chip, having automatic synthesis tools that implement logic functions have become indispensable on these architectures. Conventional synthesis approaches fail to produce satisfactory solutions for FPGAs, since the constraints imposed by the FPGA architectures are quite different. FPGA technology has, therefore, more powerful design tools and considered effective because it shortens the design cycle, provides good utilization of the device and synthesizer options i.e., choose between optimization speeds versus size of the design.

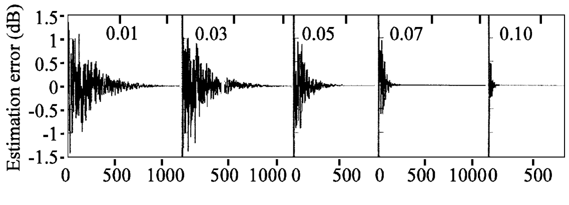


Fig. 2: Performance of adjoint LMS adaptive filter at various step size

The design is coded in Verilog HDL (hardware description language), a more generalized method of describing the behavior of logic systems than logic equations. The system is visualized as a set of black boxes called modules. The top level module is broken into successively less complex functions until the bottom level is reached (RTL level description of the function). The Adjoint LMS algorithm is simulated and examined to assess whether the simulation has achieved the desired result using Modelsim 5.8. Its equivalent timing diagram is shown in Fig. 4. for 16-bit input data.

Logic synthesis takes the circuit description at the register-transfer level and generates an optimal implementation in terms of interconnections of logic gates. Schematic capture is, probably, still most popular method of defining logic for FPGAs and many ASICs. It is a CAD system dedicated to logic design. Logic

Table 1: Mean, variance, MSE and SNR values for various step size

Mu	Variance	Mean	Mse	Snr
1E-06	0.3915	0.0133	0.3349	-24.63
6E-06	0.139	-0.0077	0.1125	-30.813
0.00001	0.0971	0.0034	0.0779	-33.325
0.00006	0.0265	0.0053	0.0216	-45.319
0.0001	0.0223	7.73E-04	0.0184	-45.043
0.0006	0.0075	-0.0039	0.0089	-55.267
0.001	0.0079	1.66E-04	0.0069	-56.947

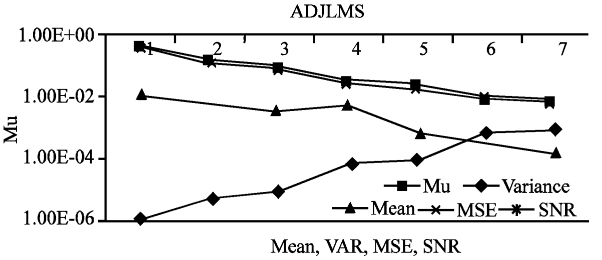
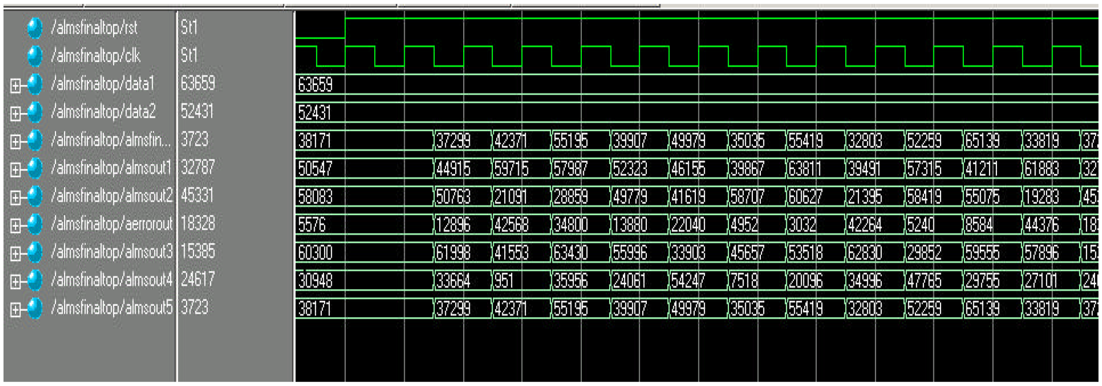


Fig. 3: Mean, variance, MSE and SNR plot for various step size


/almsfinaltop/rst St1
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/almsfinaltop/aerrorout 18328 5576 12896 42568 34800 13880 22040 4952 3032 42264 5240 8584 44376
/almsfinaltop/almsout3 15385 60300 61998 41553 63430 55996 33903 45657 53518 62830 29852 59555 57896
/almsfinaltop/almsout4 24617 30948 33664 951 35956 24061 54247 7518 20096 34996 47765 29755 27101
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Fig. 4: Timing diagram of filtered adjoint LMS algorithm

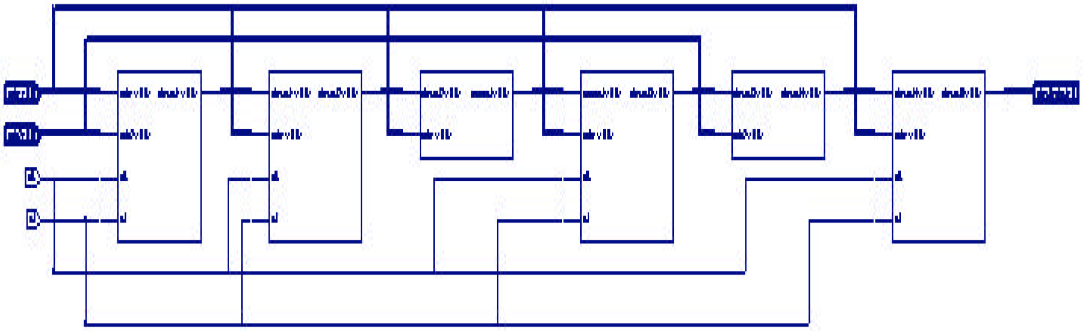

Fig. 5: Synthesis result

functions of complexity ranging from an inverter to multi-bit counters are stored in a library which describes both their functionality and a graphic symbol. The designer calls up the symbols from the library, places them on the screen of a PC or workstation and connects them with wires and busses.

The modification of the design takes place at 2 levels. At the visual level, the designer creates a visual representation of the logic which is required, in terms of familiar symbols for the components. At a level below this is a net list which defines the location of the each component on the screen and the way each is connected to the other components in the design.

The RTL description of Adjoint LMS algorithm is first optimized for an objective function such as minimum chip area, meeting the performance constraints, low power, etc. This step is called logic optimization. The optimized representation is then mapped to some primitive cells present in a library. The final implementation is in terms of interconnections of gates, functional units, registers, is synthesized in Xilinx 6.3i and implemented on a Virtex XC2VP40-6 chip is shown in Fig. 5.

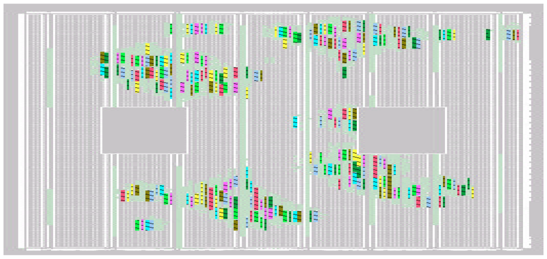

Fig. 6: Floorplanning report in FPGA

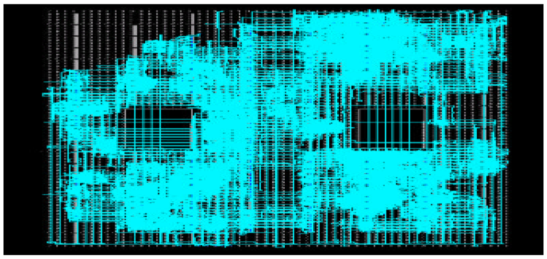

Fig. 7: Implementation report in FPGA

Table 2: Characteristics of filtered XLMS and adjoint LMS

Architecture	Registers	Adders/substractors	Multipliers	Comparators
FXLMS	520	185	97	60
Adjoint LMS	520	185	104	60

Table 3: Characteristics of filtered XLMS and adjoint LMS

Architecture	Gatecount	Power	Frequency	IOB's	Memory usage
FXLMS	453.520	873 mW	24 MHz	2400	209 MB
Adjoint LMS	476.748	798 mW	27 MHz	2400	204 MB

Floorplanning allows to predict the interconnect delay by estimating the interconnect length (Michael, 2001). The goals of floorplanning are to arrange the blocks on a chip and decide the location of the I/O pads, power pads, power distribution and clock distribution. The objectives of floorplanning are to minimize the chip area and minimize delay. The adjoint LMS algorithm is floor planned and its result is shown in Fig. 6.

The locations of various modules on the chip are determined (placement) and the interconnections of the circuit are routed between or through the placed modules. Also, the pad locations for inputs and outputs are determined in this step. The final layout is sent for fabrication and the layout for the Adjoint LMS algorithm is shown in Fig. 7.

The timing simulation data generated from Place and Route are generated to carry out the timing simulation for the final verification of the design (Meyer, 2006). Best performance is achieved by mapping the basic components to use the minimum Array-of-Slices (AoSs). The arrangement of the component's position in the Virtex device is important in minimizing the interconnect delay. The components used to implement the Adjoint LMS have been optimized for the Virtex FPGA circuit (Geoff, 1996). Characteristics comparison Table 2 and 3 for FILTERED- XLMS and Adjoint LMS algorithm is given below:

Device utilization summary of adjoint LMS

Selected device: 2vp30ff896-6		
Number of slices:	3310 out of	13696 24%
Number of slice flip flops:	659 out of	27392 2%
Number of 4 input LUTs:	6008 out of	27392 21%
Number of bonded IOBs:	49 out of	556 8%
Number of MULT18X18s:	104 out of	136 76%
Number of GCLKs:	1 out of	16 6%

CONCLUSION

In this study, a high-speed FPGA implementation of Adjoint LMS filter is presented. The algorithm has been successfully implemented on the Virtex 2vp30ff896-6 chip. The powerful design of Adjoint LMS algorithm using reconfigurable logic shortens the design cycle and provides good utilization of the device and also provides synthesizer options, i.e., chooses between optimization speed versus size of the design. As inferred from speed analysis, the Adjoint LMS algorithm, exhibits considerably more speed consumption at the RTL coding stage. The gate count, area analysis, registers, adders/subtractors, comparators, speed of multipliers and frequency of Adjoint LMS algorithm prove to be exceptional. Also, error floor and the consistency of the error are, in general, better for the Adjoint LMS algorithm compared to Filtered X-LMS algorithm. The MATLAB results also prove to be effective.

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