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New Design for FIR Filter with Optimization of Speed and Power Using ASIC

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Abstract: This study develops and demonstrates the optimization of frequency and power of proposed parallel, pipelined flipping architecture for image compression using 2-D Discrete Wavelet Transform (DWT). All the filters used in DWT such as alpha, beta, gamma and delta are computed in parallel manner. Last two filters give the output of low pass and high pass filter. Because of parallel processing of these filters, waiting for the results of first two filters is not required. Modified bough-wooley with pipelined constant co-efficient multiplier is used for signed multiplication. One level 2-D DWT with pipelining and without pipelining of FIR filters are designed and synthesized using design compiler with 0.18μm process technology. Two level with pipelining and without pipelining is designed using this new structure as well. Synthesis results of design compiler show that the speed of proposed one level 2-D DWT is increased by 44 and 2.47% of power is decreased compared to existing architectures. Hardware cost, latency of proposed structure is reduced compared with existing structures. Computation time, number of multipliers and adders required for this filter is compared with various architectures.

Key words: Application specific Integrated circuits, discrete wavelet transform, flipping architecture, logical elements, image compression, constant coefficient multiplier

INTRODUCTION

Wavelet analysis is a data processing technique with outstanding performances in time-frequency analysis. In the last decade, wavelet and wavelet based analysis have been used in a lot of diverse fields of Science and Engineering. Wavelets are categorized into two groups: continuous wavelet and discrete wavelet. They comprise a family of tasks, create from dilations and translations of a particular function called the mother wavelet (Mallat, 1989). DWT is broadly occupied in image and video compression methods due to its outstanding decorrelation properties. Specifically, many famous coders have been estimated to successfully compress images or frames processed through DWT. In addition, the DWT is occupied in JPEG2000; the new standard for image compression where the lossy and the lossless compression are employed as the default filters of 5/3 and 9/7 bi-orthogonal wavelet filters respectively (Acharya and Tsai, 2005).

ASIC design tools: DSP functions, specifically Filters (FIR) are commonly expanded into Digital Signal Processors (DSP) and Field Programmable Gate Arrays (FPGA). At the original level, FPGA design and verification tools are strongly correlated to ASIC development tools and carry out most ASIC designs are prototyped on FPGAs. ASIC design verification is done by using Cadence, Mentor graphics and Tanner EDA (Electronic design automation) tools. Cadence-Encounter Compiler proposes true top-down universal Register Transfer Level (RTL) design synthesis to accelerate silicon realization. This Compiler carried out multi-objective optimization to construct logic architectures that meet on all the objectives in a particular pass. With this optimization and hold for superior low-power design methods, compiler decreases chip power expenditure while meeting frequency goals. It distributes the most excellent speed, area and power after physical implementation of the many challenging designs (www.cadence.com, www.altera.com).

Literature review: Much architecture has been proposed for increasing the speed and reducing the power of DWT. (Madishetty *et al*., 2013) proposed a new architecture for multi encoded arithmetic integer based doubechies-4 and

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6 filters. This structure gives error free and noise free coder for multilevel image processing. (Marino, 2000) proposed architecture is based on non-separable approach and direct approach. Low power and four times higher speed of operation than other approaches is achieved by using pipelining process. A multiplexer is used for increasing the speed and reduce hardware complexity. (Liao *et al*., 2004) proposed four architectures namely dual scan and recursive for 1-D and 2-D discrete wavelet transform. Hardware utilization of these architectures is 100 and 90%. Memory buffer required for processing intermediate data are less. Lai *et al*. (2009) proposed a pipelined and parallel scanning architecture using lifting scheme. Internal buffer size required for this architecture is less and it produces two data per clock cycle. Zhang *et al*. (2010) presented a method for the structure of pipeline design for a high speed computation of the DWT.

This is attained by reducing the period of clock cycles. In order to minimize these two parameters is to optimally distribute the task of the DWT computation and to maximize inter and intra stage simultaneous and pipeline processing. Tian *et al*. (2010) described about the construction of an efficient Multi-Input/Multi-Output VLSI design (MIMOA) based on lifting scheme which attains the high processing speed constraint with the controlled raise of hardware complexity. High speed of operation can be met by using multiple row data samples are computed concurrently and the multiplexing method is used so as to reduce the hardware cost. Lee *et al*. (2012) shows that the optimization techniques used to reduce operand bit size in a Bit-Parallel (BP) architecture and to decrease iterations in a Digit-Serial (DS) architecture.

These architectures enable implementations with an important enhancement in hardware resources, execution time and precision requirements. Zhang *et al*. (2012) presented non-separable pipeline design for high speed computation of the 2-D DWT with reasonably low cost hardware resources. The speed of the computation is raised efficiently by distributing the assignment of the computations to many sub-band levels among the levels of the pipeline and harmonizing the operation of the pipeline so as to take benefits of the inter stage and intra stage processing parallelism. Darji *et al*., 2014) proposed dual scan algorithm develops the distribution of the intermediate data on different independent paths of a Data-Flow Graph (DFG). LS are implemented simultaneously and pipelining is also used to reduce the latency to Tm with a very simple control path. The architecture only needs $N^2/2$ clocks to develop an N×N image and only requires five registers for transposition. Huang *et al*. (2002) proposed line based architectures for single level and multi-level decomposition. Row wise and column wise pixels are processed simultaneously. The proposed architecture is an integration of convolution and lifting based architectures. Three generic RAM-based architectures produce high efficiency and feasibility for both 1-level and multi-level line-based 2-D DWT architectures. Wu and Lin (2005) proposed a new architecture for implementing 5/3 and 9/7 wavelet filters. Internal memory access is greatly reduced; number of pipeline registers is also reduced in the proposed architecture. Kotteri *et al*. (2006) presented a design procedure of great performance, fixed-point, multiplier less sub-bands using the bi-orthogonal 9/7 wavelet filter for Image compression. High-performance filters are intended by the researcher using multiplier less hardware where computation is carried out using shift and add after is approximating every filter coefficient as an addition or diversity of powers of two (SPT). (Martina and Masera 2009) explained a multiplier less VLSI structure for the well-known 9/7 wavelet filters. Researcher implant the 5/3 wavelet computation into the 9/7 so as to reach as much as probable to the 5/3 results to realize the 9/7 ones with a decreased number of adders. Dhandapani and Ramachandran (2014) proposed an image processing system by focusing on the lossy bi-orthogonal 9/7 Lifting Scheme (LS) supported DWT structure. This application initiates an enhanced image processing system which makes use of a low-power DWT structure beside with a log-based Floating Point Unit (FPU) and block Based Pass-Parallel SPIHT (BPS) coder. The drawback of these designs is filters because they are computed in serial manner.

Organization: In this, increasing the frequency of operation and reducing the power dissipation of bi-orthogonal 9/7 filter by using parallel and pipelining approach is discussed. All the stages of filter are computed in parallel. Only two stages out of four are sufficient for DWT computation. Two multipliers and two adders are only used for this filter process. The control circuits are not required for this process. Advantages and disadvantages of lifting scheme, Flipping Architecture (FA), Modified Flipping Architecture (MFA) and Multiplier Free Modified Flipping Architecture (MFMFA) are discussed and compared with the results of the proposed architecture in the following sections.

For the computation of 2-D DWT, 2's complement multiplications are required. In the literature (Parhi and Nishitani, 1993; Parhi, 1999; Hu and Parhi, 2013). The BW method has been studied with carry save adder, ripple carry adder and many algorithms. These algorithms are ineffective in speed, area or both when one of the

operand is fixed. A new multiplier algorithm denoted as Modified Baugh-Wooley pipelined constant coefficient multiplier (MBW-PKCM) is proposed and implemented in a PPFA on ASIC. For an N-bit number, two's Complement Multiplier (C2CM) needs N minus 1/4 arrays of four inputs LUTs. MBW method requires N divided by four arrays of four input LUTs. The size of an array is equal to the number of product bits. The 2's complement block increases the number of LUT array area and multiplication time for the C2CM. However for MBW, the amount of LUT array is identical as that required for the first scheme. The PPFA with Bough wooley requires four percentage less area compared to that of sign extension scheme. In 2-D DWT, filter coefficients are constant. Hence, MBW which combines the pipelined KCM is used in this study. One level and two, level 2-D DWT of proposed architecture is implemented using Encounter RTL Compiler (Cadence TSMC) 0.18 μm process technology. The computation time required for PPFA is reduced into Tm+Ta where Tm is the time required for multiplication and Ta is the time required for addition. Hence, PPFA is a more efficient architecture and it is best suited for 2-D DWT implementation. Results of proposed architecture are compared with existing architectures and state-of-the-art is given in Annexure-1 (Parhi, 1999; Cheng and Parhi, 2008; Sun *et al*., 2013).

Literature review: In this study, existing techniques which are used for the implementation of 2-D DWT has been analyzed.

Features of LS: The primary characteristics of LS based DWT method are to split the HPF and LPF (low pass and high pass filter) wavelet filters into a series of smaller filters. LS based DWT decreases the memory necessities and messaging between the processors when the picture is divided into small blocks. In the LS for a sub band structure with the low pass and high pass filters of 9/7 wavelet filter, respectively, the odd and even input data are processed by five blocks [α, β, γ, δ, ξ_(ξ 1 and ξ 2)] as shown in Fig. 1. ξ 1 and ξ 2 are scaling blocks. The primary drawback of LS is the longer critical path.

Flipping based DWT: The FA (Cheng *et al*., 2007; Huang *et al*., 2004) is implemented by taking the inverse of lifting coefficients. Conventional LS-based architectures require fewer arithmetic operations and more pipeline registers; hence this architecture has longer critical paths so that it causes a severe time delay problem than convolution-based ones. Timing accretion is effectively

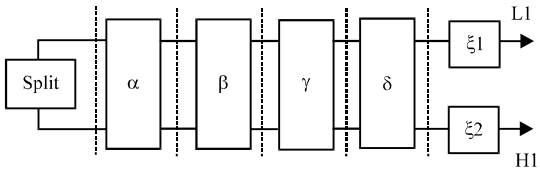

Fig. 1: Block diagram of Flipping Architecture (FA)

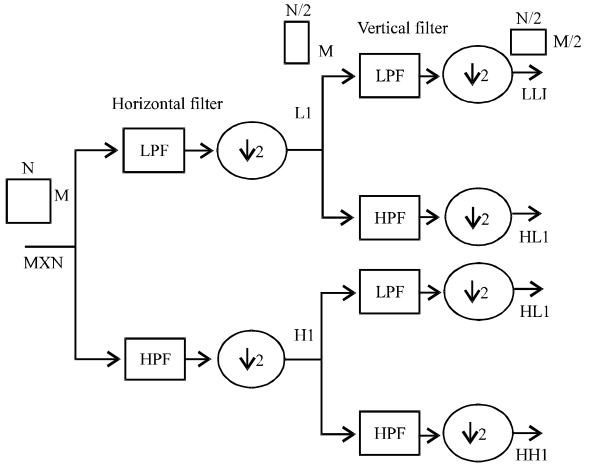

Fig. 2: Subband decomposition of filter bank approach

reduced by multiplying the reverse coefficient for all edges on the feed-forward cutset by selecting proper multiplier in the FA. So, the critical path of flipping is reduced from 2Tm+3Ta to Tm+3Ta. The advantage of flipping structure is, additional multipliers will not be required if the computing units of LS are all flipped.

Advantages and disadvantages of FA: FA requires four multipliers and eight adders compared with LS. Disadvantages of FA are one is serial operation and another one is multipliers and shifters. These are reducing the frequency of operation of the FA in Fig. 2.

MATERIALS AND METHODS

Modified flipping architecture: The major difference between LS and FA is shifters. Many shifters are used to design FA. So, shifters and adders are reduced according to the following calculations. Modified Flipping Architecture (MFA) is implemented using MBW-PKCM technique. Twelve bit precision is used for the multiplier coefficients to obtain better resolution. An alpha block of MFA is similar to conventional FA. The input data of beta block is right shifted by four times in the FA.

Similarly, input data of gamma and delta are right shifted by one time (Parvatham and

Seetharaman, 2012, 2014a,b). The following calculations are made in MFA to reduce the shifters of filters in FA.

Beta block:
$1/2^4+1/2^4 = 2/2^4 = 1/2^3$
Number of shifters reduced from 4-3:

Gamma block:
1/2+1/2 = 2/2 = 1

Delta block:
1/2+1/2 = 2/2 = 1

So, shifting is not required for gamma and delta blocks. In MFA, right shifting is not required for both gamma and delta blocks. Only one shifter is required for beta block. Hence, the number of adders required for MFA implementation is greatly reduced. The existing method requires eight adders, four multipliers and many shifters. For MFA, five adders, only one shifter and four multipliers are required. The hardware requirement is greatly reduced in MFA. The disadvantage of this structure is multipliers. It reduces the speed and occupies more area. So, multiplier free structure is needed to reduce the delay and area.

Multiplier free modified flipping architecture

Optimize multiplication: The important part of many VLSI design tasks is the computation of a variable by a group of constants. The efficient implementation of these computations can direct to important enhancement in different design parameters like area or power consumption. Hardware cost is eventually measured in terms of the number of logic elements used. Critical path delay or the number of clock cycles that it obtain from the time that an input go into the system to the time that the consequent output exits the system is also important. The primary computation in FIR filters is coefficient multiplications which is developed using shift and add, out of which the addition process leads the difficulty because shifts are less complex. Many adders are used to add the sum of the partial product terms obtained when the input signal is computed by the coefficients and the latency path lengths of the computation operation are the two metrics that decide the difficulty of FIR filters. Therefore, the techniques that minimize the complexity of computation in FIR filters focus on decreasing the number of logical elements used to develop the multipliers.

Multiplier free concepts: Multiplier-free concepts are applied in to MFA for reducing hardware cost and latency. So, it is called Multiplier Free MFA (MFMFA). KCM is not essential for this architecture. As an alternative of multiplier, shifters and adders are used in MFA is called MFMFA explained by Parvatham and Seetharaman (2014a). Every filter co-efficient is multiplied by the input data in the existing structure. So, the input data is shifted based on the values of the filter coefficient. The input data are variable and filter coefficients are constant. The only disadvantage of this architecture is serial operation. A fully parallel, pipelined FIR filter is implemented in an ASIC can operate at very high data rates, making ASIC ideal for high-speed filtering applications.

Proposed parallel and pipelined flipping architecture

PPFA with modified bough-wooley multiplier: Main aspire of this research is the implementation of a well-organized method for the design of optimal VLSI architecture using 2-D DWT. For 2-D image data, a single level 2-D DWT requires two passes of one-dimensional (1-D) transforms, i.e., a perpendicular and a parallel. At every pass, a 1-D transform is carried out on each row or column of the data. Therefore, an image with N rows and M columns of pixels, 2-D transform would require 2MN transform operations. Each filter has 5 blocks shown in Fig. 1.

The LL1 is the coarse form of input image. The input data are sent through the 2 levels of analysis filters. They are initially progressed by the low pass and high pass parallel filters and are divided by two to get N×M/2 matrices L1 and H1. Subsequently, the outputs (L1, H1) are functioned by low pass and high pass perpendicular filters to get four N/2×M/2 transform coefficient matrices. One of these four matrices denoted as LL1 characterizes a coarse estimation of the novel image. For the second level of 2-D DWT, LL1 component is progressed by both parallel and perpendicular filters and sub-sampled to get another four matrices Low Low2, Low High2, High High2 and High Low2. This is continued up-to the desired stage of sub-band structure is achieved (Parvatham and Seetharaman, 2012).

Each horizontal and vertical filter have four blocks such as alpha, beta, gamma and delta are connected sequentially in Flipping Architecture (FA) shown in Fig. 1. Every block has to wait for the results of the previous block for the computation of filter operation. Likewise, final block in a flipping architecture is waiting for the results of previous three blocks for computation. In the proposed architecture of PPFA, every block is computed in parallel manner. This is achieved by multiplying every block with succeeding blocks. Three stages of pipelining are used for increasing the speed of operation. So, this proposed architecture is called as

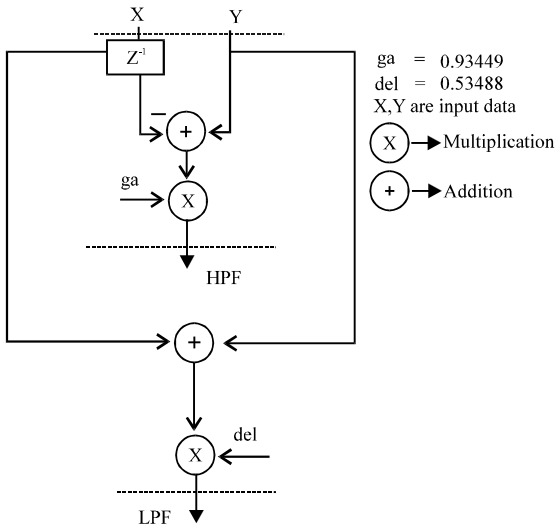

Fig. 3: Internal architecture of PPFA (horizontal filter)

Parallel and Pipelined Flipping Architecture (PPFA). Speed of non-pipelining architecture is less compared to pipelining structures. But, area occupied by non-pipelining is less compared to pipelining architectures.

In PPFA, all the blocks can be computed in parallel shown in Fig. 3. Horizontal filter of proposed PPFA is shown in Fig. 3. Same structure is also applicable for vertical filters. Equation 1 is derived from the lifting coefficients:

$$\begin{bmatrix} \frac{1}{a} & 1+z^{-1} \\ 0 & \frac{1}{a} \end{bmatrix}\begin{bmatrix} \frac{1}{16b} & 0 \\ \frac{1+z}{16} & \frac{1}{16b} \end{bmatrix}\begin{bmatrix} \frac{1}{2c} & \frac{1+z^{-1}}{2} \\ 0 & \frac{1}{2c} \end{bmatrix} \begin{bmatrix} \frac{1}{2d} & 0 \\ \frac{1+z}{2} & \frac{1}{2d} \end{bmatrix}\begin{bmatrix} 64abcdk & 0 \\ 0 & \frac{64abcd}{k} \end{bmatrix} \quad (1)$$

The first matrix of Eq. 1 is multiplied with the even and odd input (x, y) data of image Eq. 2. The resultant is-0.6304y+2x gives the output of alpha block. Pipelined registers are included with this architecture. Then output of second equation is multiplied with the second matrix of Eq. 1. The result of this multiplication is -0.0788y+0.99367x which gives the output of beta block. Similarly, the output of every matrix multiplication is multiplied with the consequent matrixes of Eq. 1. Equation 4 gives the output of both gamma and delta blocks. Last matrix of Eq. 5 is the result of low pass filter and high pass filter. So from the Eq. 2-5: alpha, beta, gamma and delta values can be computed in a parallel manner.

$$\begin{bmatrix} \frac{1}{a} & 1+z^{-1} \\ 0 & \frac{1}{a} \end{bmatrix}\times\begin{bmatrix} y \\ x \end{bmatrix}=\begin{bmatrix} -0.6304y+2x \\ -0.6304x \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} \frac{1}{16b} & 0 \\ \frac{1+z}{16} & \frac{1}{16b} \end{bmatrix}\times\begin{bmatrix} -0.6304y+2 \\ -0.6304x \end{bmatrix}=\begin{bmatrix} 0.74367y-2.35938x \\ -0.0788y+0.99367x \end{bmatrix} \quad (3)$$

$$\begin{bmatrix} \frac{1}{2c} & \frac{1+z^{-1}}{16} \\ 0 & \frac{1}{2c} \end{bmatrix}\times\begin{bmatrix} \frac{1}{2d} & 0 \\ \frac{1+z}{2} & \frac{1}{2d} \end{bmatrix}\times \begin{bmatrix} 0.74367y-2.35938x \\ -0.0788y+0.99367x \end{bmatrix}=\begin{bmatrix} 0.3680y-0.3680x \\ 0.291991y+0.2920x \end{bmatrix} \quad (4)$$

$$\begin{bmatrix} 64abcdk & 0 \\ 0 & \frac{64abcd}{k} \end{bmatrix}\times\begin{bmatrix} 0.3680y-0.3680x \\ 0.291991y+0.2920x \end{bmatrix}=\begin{bmatrix} 0.93449y-0.93449x \\ 0.53488y+0.53488x \end{bmatrix} \quad (5)$$

One level of PPFA and low pass, high pass filters are designed using the last equation of Annexure 1. The proposed architecture PPFA of 1-D DWT is shown in Fig. The 3. 1-D DWT consists of one low pass and one high pass filter. One level 2-D DWT is computed using Fig. 4. One level 2-D DWT consists of one horizontal and two vertical filters. Each filter has five blocks such as α, β, γ, δ, ξ. These filters are operated in a parallel manner. The advantage of this method is reducing the computation time and power. The speed of the architecture is greatly improved by establishing pipelining for each and every block and LUT's. MBW multiplier is used for multiplying inputs with signed and unsigned filter coefficients. The advantage of this multiplier is to multiply sign bit up to 32 bits. Delay of each stage is reduced by using PKCM. LUT's are used to store the values of filter coefficients.

RESULTS AND DISCUSSION

Implementation results of one level and two level 2-D DWT: The flow diagram of one level 2-D DWT using proposed architecture Eq. 5 is shown in Fig. 4. The size of the input image is 512×512. Sizes of sub images are 32×32. Overlapping of images is not required for this process. For the horizontal filters, even and odd inputs are the size of 512×12. The result of horizontal filter is divided into two 256×256 pixels. Output of two level 2-D DWT is 64×64.

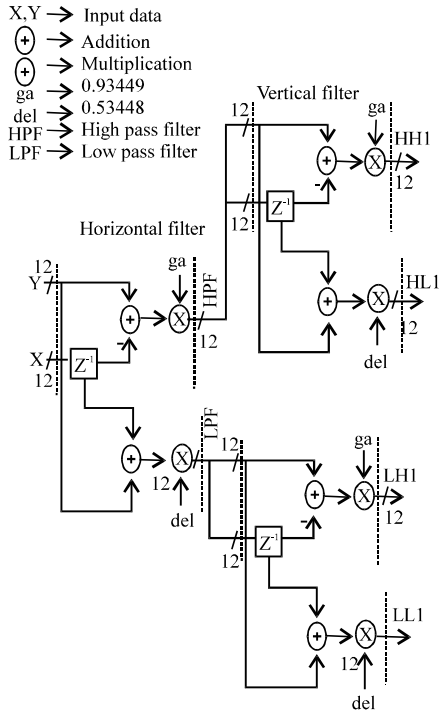

Fig. 4: One level 2-D DWT using PPFA

Implementation results using 0.18 µm process:

The 2-D DWT is implemented using cadence 0.18 µm process technology. The VERILOG HDL language is used to describe the functionality of the circuit and after the circuit is described in HDL, functionality is verified and compiled using Encounter RTL. Comparisons of all the architectures using TSMC 0.18 µm standard cell library are shown in Fig. 5 and 6. For one level 2-D DWT, frequency of operation of PPFA is raised by 44% compared with the FA, 39.95% raised compared with MFA, 23.1% raised compared with MFMFA, 11.9% raised compared with non-pipelining architecture. Power dissipation is reduced by 2.47% compared to FA, 7.49% reduced compared with MFA. Hardware occupied by these structures is compared in Table 1 and 2. Area occupied by the non-pipelining structures is less compared to pipelining structures. The proposed architecture is implemented using non-pipelining and compared with the results of pipelining. PPFA is compared with various structures are given in Table 3. Power and computation time required for proposed one is very less compared with other structures shown in Table 3. Six multipliers and six adders only required for one level 2-D DWT of PPFA. For the purpose of verification, the proposed structure is also verified using standard JPEG images such as Lena, Houses, Light house and Mandrill shown in Fig. 7 by using Matlab. Peak signal to noise ratio of Lena image of one level 2-D DWT

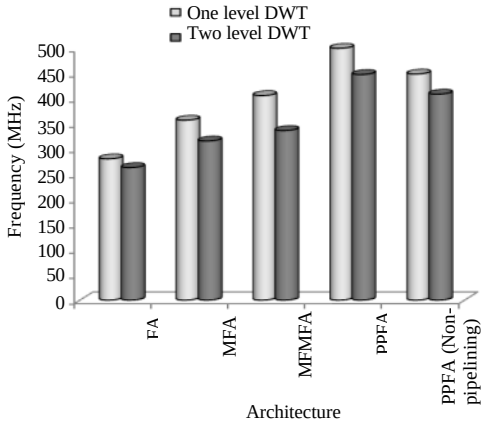

Fig. 5: Frequency comparison of different architectures

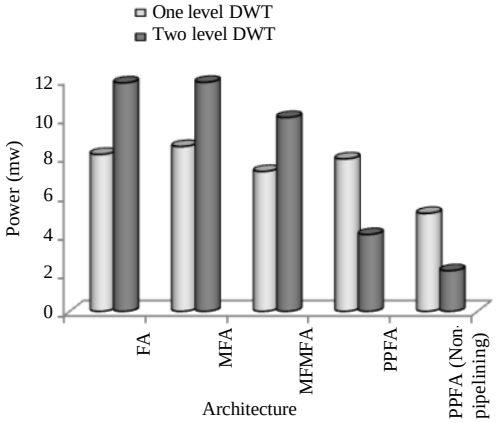

Fig. 6: Comparison of power of different architectures

Table 1: Comparisons of FA, MFA and MFMFA using 0.18µm process

	One level 2D DWT			Two level 2D DWT		
Description	FA	MFA	MFMFA	FA	MFA	MFMFA
Area	386456	384426	364507	556223	550715	522841

Table 2: Comparisons of PPFA with pipelining and without pipelining using 0.18 µm process

	One level 2D DWT		Two level 2D DWT	
Description	PPFA	PPFA with non-pipelining	PPFA	PPFA with non-pipelining
No of cells	53346	53069	90170	89606

is 41.39. Compression ratio of two level 2-D DWT is 64:1. Satellite images and medical images can be compressed by using this compression technique.

CONCLUSION

In this study, parallel and pipelined flipping architecture and non-pipelining is implemented using one

Fig. 7: Output images of one level 2-D DWT; a) Lena; b) Houses; c) Light house and d) Mandrill

Table 3: Comparision of various parameters of proposed architecture with existing structures for one level DWT (512×512 image)

Architectures	Multiplier	Adder	Power (mw)	Time (ns)	Computation time
Cheng *et al.* (2007)	12	16	-	-	Tm+2Ta
Lai *et al.* (2009)	10	16	8.973	11.060	Tm
Xin *et al.* (2011)	6P	8P	13.400	15.520	Tm+2Ta+t1
Xin *et al.* (2011)	6P	8P	18.400	15.630	Tm+2Ta+t1
Mohanty and Meher (2011)	4.5P	8P	11.600	16.950	Tm+2Ta+t1
Mohanty and Meher (2011)	4.5P	8P	12.400	17.630	Tm+2Ta+t1
Mohanty *et al.* (2012)	4.5P	8P	8.700	16.660	Tm+2Ta
Mohanty *et al.* (2012)	4.5P	8P	9.000	15.980	Tm+2Ta
FA	12	24	8.131	3.564	Tm+3Ta
MFA	12	15	8.540	2.799	Tm+2Ta
MFMFA	0	36	7.250	2.462	2Ta
PPFA (proposed)	6	6	7.900	2.000	Tm+Ta
PPFA (non pipelining) (proposed)	6	6	5.070	2.227	Tm+Ta

P = Image block size; t1 = time delay of multiplexer

level and two level 2-D DWT. The proposed FIR filter architecture is implemented in CMOS 0.18μm process technology. From the ASIC implementation results, it is verified that this structure of one level 2-D DWT operated with higher speed by 44% compared with the FA. The power dissipation is also reduced by 2.47%. Hardware comparison of both one level and two level are given in Table 1 and 2. State-of-the-art is given in Table 3. MBW-PKCM is used for increasing the speed of operation. Power required for PPFA is very less. Latency of PPFA is also very less. Both one level and two level of proposed architectures are implemented using non-pipelining. Pipelining architectures are better than non-pipelining. For the purpose of verification, the proposed structure is also verified using MATLAB. The proposed structure is also verified using standard JPEG images such as Lena, Houses, Light house and Mandrill shown in Fig. 7 by using MATLAB. Peak signal to noise ratio of Lena image of one level 2-D DWT is 41.39. Compression ratio of two level 2-D DWT is 64:1.

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