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Z-TCAM: An Efficient Memory Architecture Based TCAM

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Abstract: Ternary Content Addressable Memory (TCAM) is normally utilized as a part of rapid inquiry concentrated applications, for example, ATM switch, IP channels. Consequently, presently Z-TCAM is presented which copies the TCAM usefulness with SRAM. It has a few disadvantages, for example, low versatility, low stockpiling thickness, moderate access time and high cost. Be that as it may this system proposes a novel memory structural planning of existing Z-TCAM utilizing STT-RAM. Subsequently, the range delay and force are lessened by utilizing STT-RAM. The point by point usage results and power estimations for every outline have been accounted for altogether using modelsim and quartus tool. Power measurements for each design have been reported thoroughly.

Key words: Ternary Content Addressable Memory (TCAM), Static Random Access Memory (SRAM), Spin Torque Tunnel RAM (STT-RAM), Magnetic Tunnel Junction (MTJ), rapid

INTRODUCTION

Ternary Content Addressable Memory (TCAM) is an development of arbitrary Access Memory (RAM) however, not at all like RAM, TCAM gives access to put away information by substance as opposed to by a location and yields the match address. Since, TCAM can store couldn't care less state (x) which can be coordinated to both 0 and 1 amid an examination operation, numerous matches may happen. A common CAM contrasts inquiry key and all the put away words in parallel and returns the location of the best match. Since, TCAM gives rapid parallel inquiry operation, it has a wide utilization of applications, for example, it can discover its applications in system switches, interpretation look-aside cushions in microchips, information pressure, ongoing example coordinating in infection recognition, interruption location frameworks, quality example seeking in bioinformatics and picture handling.

The essential use of TCAM is in system frameworks where to analyze the destination location of approaching parcel against the put away addresses and forward the bundle to the proper yield port. In spite of the fact that CAM innovation presents a noteworthy point of preference of a solitary clock cycle correlation over standard RAM, yet it additionally has weaknesses. TCAM is not subjected to the exceptional business rivalry found in the RAM business sector but then to pick up a considerable piece of the overall industry. The expense of TCAM is around 30 times more for every piece of capacity than the SRAM cost. For giving parallel hunt operation, TCAM needs examination hardware in every cell which directs that CAM thickness slacks RAM thickness. The correlation hardware in every cell makes TCAM costly as well as adds many-sided quality to the TCAM structural engineering. The additional rationale and capacitive stacking because of the enormous parallelism protract the entrance time of TCAMs which is >3.3 times longer than the SRAM access time recognize a few read execution bottlenecks. To proposed in scaled STT-RAM cells. Investigation of the corresponding increments in detecting postpones and read mistake rates and show that differential detecting is a reasonable answer for minimize these effects as innovation hubs scale. Utilizing a proposed runtime configurable great access mode memory cell show for a situation concentrate how differential access can give superior to anything 10% execution and execution for every watt change over the best in class STT-RAM store plans in 22nm innovation while diminishing aggregate force utilization contrasted and the customary SRAM stores by 34%.

TCAM have some difficulty to degrade the efficient usage of TCAM. The major drawbacks exposed are power consumption, complex circuitry, low yield and low scalability. The equivalent searching nature of TCAM leads to high power expenditure in huge size chip and large power expenditure degrades chip reliability and affects the chip package cost. For example, an 18–Mb TCAM operation at 250 Million Searches Per Second (MSPS) consumes 15 W. Many researchers have been proposed more than a few low power methods for TCAM power expenditure reduction. At architectural level, proposed Cache-CAM (C-CAM) to decrease the power

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expenditure relation to cache-hit rate but for large hit rate have to increase the cache size and it will be increase the cache power. Proposed ones-count Pre computation-Based CAM (PBCAM) achieves low-power, low price, small-voltage and high dependability features but requires special memory cell design for reducing power consumption.

Existing works: Keeping in mind the end goal to enhance power utilization and execution of CAM cells, different configuration improvements have been completed at cell, framework engineering and coding levels in CAM plan. For the traditional excess components, a whole repetitive line (section) is utilized to supplant the broken line (segment). Rather than supplanting faulty cells with a whole CAM word, the piece based methodology is proposed by Shyue-Kung Lu in 2008. Every line of the CAM cluster is partitioned into line squares. Two extra words (SR0, SR1) are included into this CAM array. It really goes about as extra for broken cells additionally it needs exchanging rationale which expends more power.

Match line is one of the key structures in ZTCAMs. In the technique Scott Beamer and Mehmet Akgul in 2009 the NOR cell and NAND cell are utilized to develop a ZTCAM match line. In this strategy, they joined the current race plan with precomputation and particular precharging. A search cycle works in three stages: searchline pre-charge, matchline precharge and matchline evaluation. There is a potential charge-sharing issue and a bring up in the force utilization because of the hunt line precharge.

Tyshchenko and Sheikholeslami (2008) presents a Match-Line (ML) sensing scheme that distinguishes a match from a miss by first shunting every ML with a fixed negative resistance then, exciting the MLs with an initial charge and subsequently observing their voltage developments. It is known that the voltage on the matched ML will grow to VDD as in an unstable system whereas the voltage on a missed ML will decay to zero as in a stable system. Be that as it may, energy utilization is more critical in this method.

The match-line architecture Baeg (2008), the match line in each TCAM word is apportioned into four segments and is specifically pre-charged to decrease the match-line power utilization. The in part charged match lines are assessed to decide the last compared result by sharing the charges kept in different parts of the apportioned segments. This approach decreases the match-line power utilization by lessening successful capacitor stacking and voltage swing at match lines. The segmented design additionally improves operational speed by assessing numerous segments in parallel and by overlapping the pre-charging and evaluation stages.

In this approach Ullah *et al*. (2015) searching is done by verifying MSB bits of by breaking the match-lines based on MSB into several segments. When, the stored words fail to match in their corresponding segments, the search operation is discontinued for its segments. In this memory, partition scheme is consolidated by validating operating segments of ZTCAM. Multi partitioning of TCAM table Hybrid Partitioning (HP) is a combined name given to vertical divider and horizontal partitioning of the conservative TCAM table. This technique experiences low adaptability, low stockpiling thickness, moderate access time and high cost.

MATERIALS AND METHODS

Proposed work: Spin-transfer torque technology is one of the leaders among rising innovations for capacity. Its operation is based on attractive properties of extraordinary materials whose attractive introduction can be controlled and detected utilizing electrical signs. A STT-RAM cell utilizes a Magnetic Tunnel Junction (MTJ) to store parallel information. A MTJ comprises of two ferromagnetic layers and one passage obstruction layer. The two ferromagnetic layers are known as the reference layer and the free layer. The attractive course of the reference layer remains settled while the attractive heading of the free layer can be parallel or hostile to parallel, which is utilized to speak to the binary. Similar to the DRAM cell, the STT-RAM cell likewise has an entrance transistor that associates the capacity gadget and the bitline. In any case, not quite the same as Measure, the flip side of the capacity gadget is not associated with ground; rather, it is associated with the sense line. Figure 1 demonstrates a STT-RAM cell (Zhang *et al*., 2015). Like the DRAM cell, the STT-RAM cell likewise has an access transistor that associates the capacity device and the bitline.

The building block of STT-RAM is the Magnetic Tunnel Junction (MTJ) which contains two synthetic ferromagnetic layers (pinned and free layer) and one MgO presented channel barrier layer as shown in Fig. 1 (Chen *et al*., 2010). The magnetic direction of the pinned layer is fixed while the magnetic direction of the free layer can vary through the application of an external electromagnetic field or spin-polarized current through that layer. When the magnetization directions of the two ferromagnetic layers are similar, the MTJ is in its small-resistance state. In contrast, when the directions of the two layers are anti-parallel, the MTJ resistance is high. The low and high MTJ resistances can be used to represent logic values.

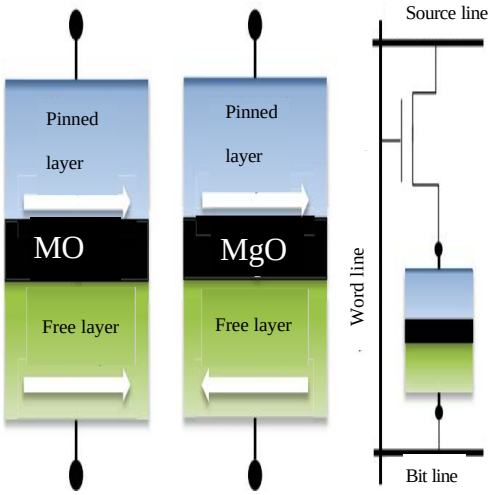

Fig. 1: Illustration of an MTJ and STT-RAM cell

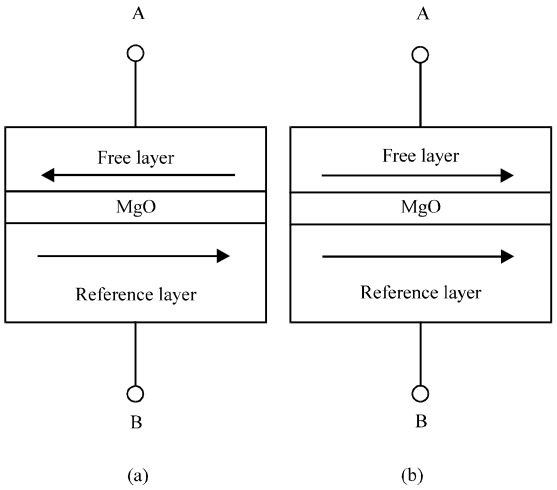

Fig. 2: MTJ structure; a) Anti-parallel (high resistance) and b) Parallel (low resistance)

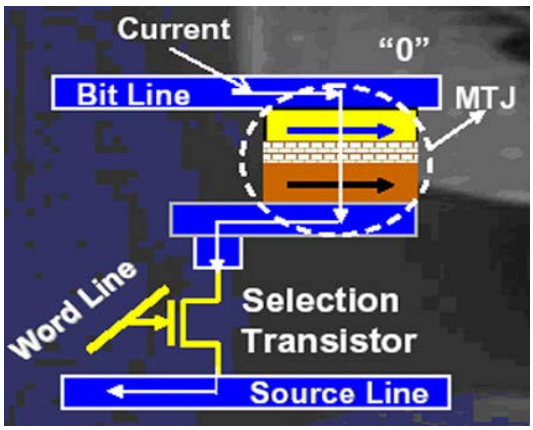

Fig. 3: Read and write mechanism in STT-RAM

In a typical STT-RAM cell shown in Fig. 1, MTJ is connected with one nMOS transistor which serves as access controller. The basic structure of typical STT-RAM memory cell is depicted in Fig. 1. It has 1 transistor (NMOS) connected in series with MTG; interconnects connected to the MTJ (bit line); interconnects of the source of transistor(source line) and interconnect of the gate (word line). One memory cell corresponds to one bit; multiple cell arrays construct a memory storage device. The transistor is used to provide the switching current density to the MTJ and used to select a particular memory cell. A memory device that is based on STT effect is of random access type, thus, it is normally referred as STT-RAM. In STT-RAM, the current density is the crucial parameter for writing a bit not current.

The reading mechanism of STT-RAM is similar tunneling mechanism. Parallel magnetizations configuration has lower resistance and thus, a lower voltage output (voltage is proportional to resistance), corresponding to a '0' state. Antiparallel configuration has a higher resistance or voltage output giving a '1' state as shown in Fig. 2.

Figure 3 shows the read and write is mechanism. During the read operation, the word line is selected and a voltage is applied to the bit line such that a current density of magnitude less than the switching current density is supplied. The writing mechanism in STT-RAM follows the current-induced magnetization switching. When a current density larger them critical current density flows from the free to fixed layer (electrons in opposite direction).

This is a '0' state because parallel magnetization has low resistance. If the current flows from the fixed to free layer, the magnetizations will be antiparallel. The corresponds to a '1' state '1' and '0' constitutes the binary states for storing information. During the write operation, a bit is selected by selecting the word line. Then, either the bit line or the source line of a selected column is positively biased. The maganetization of the free layer can be made either parallel or antiparallel with respect to the fixed layer, by changing the current direction either from source line to bit line or vice versa. The MTJ in a STT-RAM cell is planned such that, even under the most elevated working temperature conditions, it takes no <10 years for warm aggravations to irritate the polarization put away in the intersection.

Table 1 exhibits the advantages of STT-RAM over the all other memory types. In this way, for all handy purposes, STT-RAM is thought to be non-unstable, i.e., it holds the put away information uncertainly with no

Table 1: Comparison of memory technologies

Memory types	SRAM	DRAM	Flash	STT-RAM
Non-volatile	No	No	Yes	Yes
Cell size	5-120	6-10	50	2-20
Endurance	10^{16}	10^{16}	10^{5}	$<10^{16}$
Write power	Low	Low	Very high	Low
Other power consumption	Current leakage	Refresh current	No	No
High voltage required	No	2V	16-20V	<1.5V

force source. Its non-volatility Kultursay *et al.* (2013) likewise suggests that the put away information need not be invigorated occasionally; consequently, STT-RAM has no revive power. Likewise, power consumption is less for both read and write operation. Other power consumption like leakage current, refresh circuit is also avoided in this case.

The exhibit read operation in STT-RAM is nonde structive. Perusing the information put away in a STT-RAM cell requires a little measure of current to move through the MTJ which does not exasperate the put away information. In this manner, no extra inertness to recuperate the information is required. When the information is detected by the sense speakers, it can be duplicated to a line support that is decoupled from the sense speakers. This line cradle association is not quite the same as that of DRAM where the same coupled inverters are utilized for detecting and buffering. Accordingly of this decoupled design, STT-RAM sense enhancers and line cushion can work freely. This prompts a change in the way push cradle operations are taken care of in STT-RAM. A write operation is performed exclusively on the line cushion and does not proliferate through the column cradle into the memory cluster.

RESULTS AND DISCUSSION

The design is modeled in modelsim 6.4a where the program is coded and output is simulated. Figure 4 is the Register Transfer Level (RTL) view of a single memory cell. Likewise, totally 16 memory cells are present.

Initially, all the memory are written and then read operation consequently. When all the memory cells are written the search operation is perfomed. The address line is 4 bit and match line 16 bit. When a data is given as input it searches the data in the all memory cell and return the address as output where match occur. Figure 5 shows the overall architecture of the design. Total 16 memory cells are present. If multiple result is found in output means a fail. The simulated result is as depicted in Fig. 6. The proposed work is simulated in modelsim 6.4a. During the reset high there will be no output. Then, afterwards the reset signal is set as '0' state the synchronisation. Intially clock pulse is set and reset signal is given as high

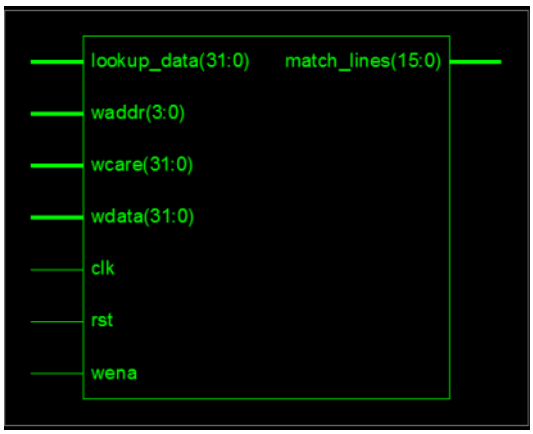

Fig. 4: The RTL of a single cell

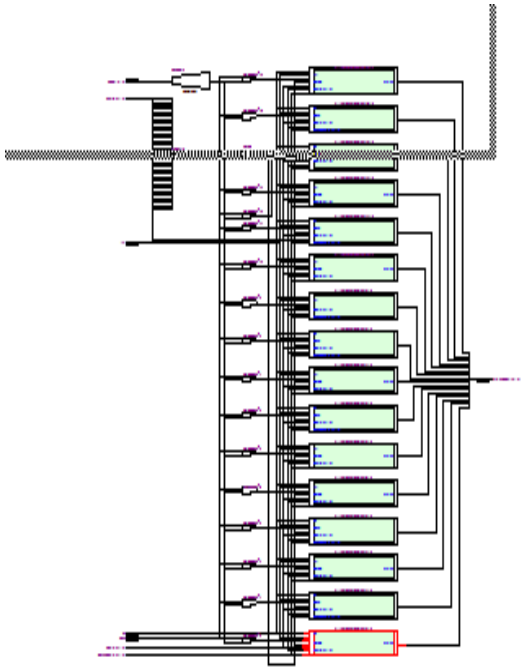

Fig. 5: The RTL view of proposed work

to have a proper synchronisation between all the signals will happen and only during the clock signal high to low transaction(1-0) the signal gets activated and the search operation will happen. All the memories are written and then only data is given and output will be taken. In Fig. 6, first 2 clock pulse the reset is high then for next 4 clock pulse write opertiontake place and remaining clock pulse search operation haappens. An extra bit "fail" is included for any mismatches or fail operation. The power, area and time all are calculated using quartus II in which cyclone III family is selected for implementation. STT-RAM) for giant size TCAM. The projected one is simply composed in

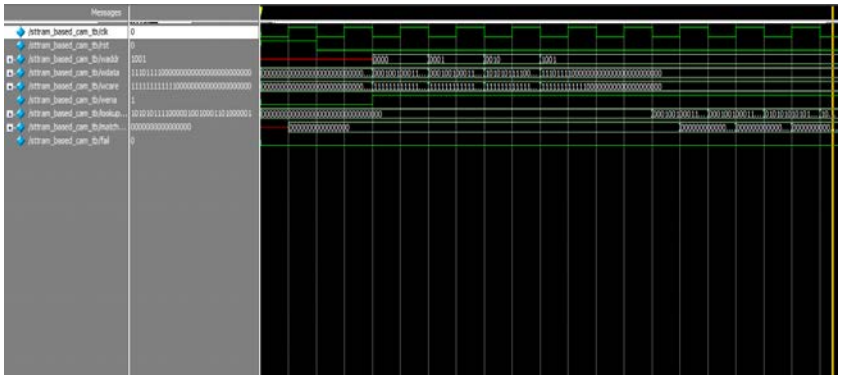

Fig. 6: Waveform of Z-TCAM architecture

Flow Summary

Flow Status	In progress - Sat Feb 20 00:12:53 2016
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	sttram_based_cam
Top-level Entity Name	sttram_based_cam
Family	Cyclone
Met timing requirements	N/A
Total logic elements	1,195 / 4,000 (30 %)
Total pins	119 / 249 (48 %)
Total virtual pins	0
Total memory bits	0 / 78,336 (0 %)
Total PLLs	0 / 2 (0 %)
Device	EP1C4F324C6
Timing Models	Final

Fig. 7: Output of space analysis

VHDL. The Z-TCAM is less complicated and simply ascendible (owing to simple measurability of surroundings and also the feasibleness has been incontestable with success. This speed is a lot of beyond the speed of classical TCAM. The projected system output of power and space analysis is given in Fig. 7 and 8.

In Fig. 7, the total pin used is only 48% which reduces the power consumption considerably. And, also uses 30% of total memory devices. Both are lesser than Sram based design.

STT-RAM is preferred than all other memory technology because of its low power consumption only, The power is also calculated with the quartus II software. The power result is shown in Fig. 8. The cyclone III family is used where the device EP1C4F324C6 power calculation always deals with two power-static and dynamic. Static power is power expended while there is no circuit movement. Dynamic power is power devoured while the inputs are dynamic.

Figure 9 depicts the comparison of SRAM and STT-RAM based ZTCAM design based on its power calculation.The thermal power of both technique varies with small value only. But, core static power is less for SRAM and I/O thermal power is less for STT-RAM design. For both, the core dynamic power is approximately zero.

Figure 10 shows the timing analysis of STT-RAM based design. In that clock time that is frequency can be also known. The clock frequency plays an important role in every working.When compared the time constraints of both SRAM and STT-RAM it is clear that some value changes.

The timing is calculated using timing analyzer in quartus II software. All logical devices will have a best case and worst case timing. Depending on its time casing only its performance will be estimated.

PowerPlay Power Analyzer Summary

PowerPlay Power Analyzer Status	Successful - Sat Feb 20 00:11:41 2016
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	sttram_based_cam
Top-level Entity Name	sttram_based_cam
Family	Cyclone
Device	EP1C4F324C6
Power Models	Final
Total Thermal Power Dissipation	60.04 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	60.00 mW
I/O Thermal Power Dissipation	0.04 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Fig. 8: Output of power analysis

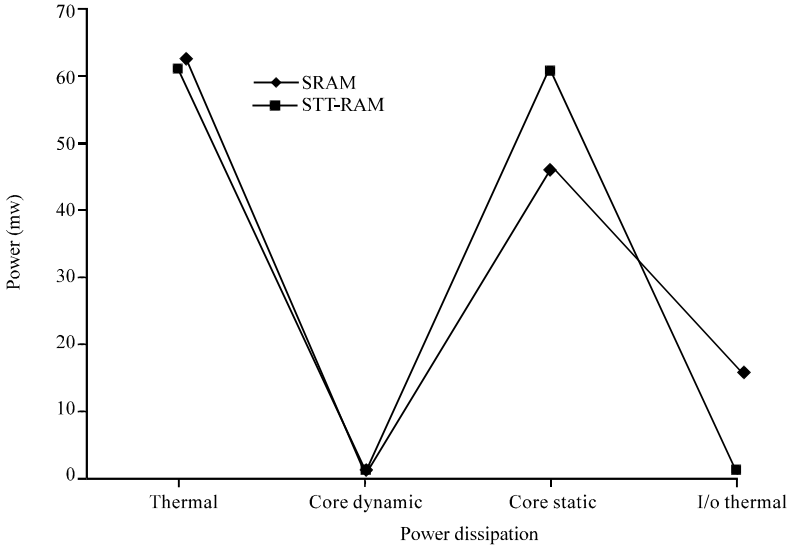

Fig. 9: Comparision of power in SRAM and STT-RAM

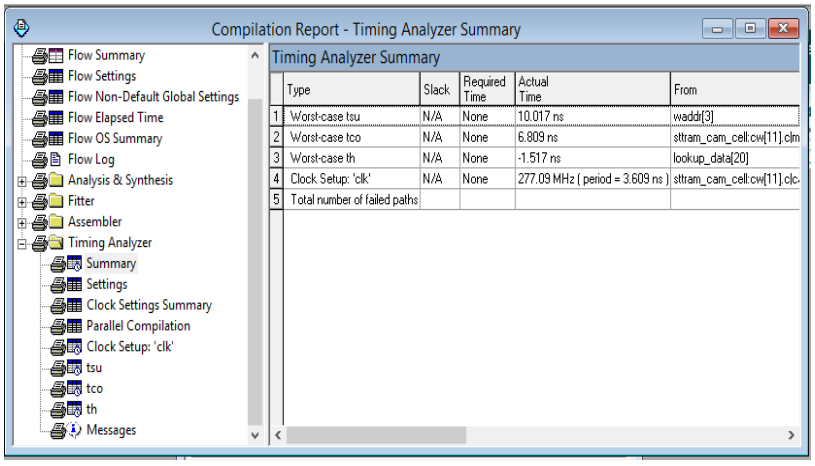

Fig. 10: Output of time analysis

Table 2: Time constraint comparison

Cases	SRAM	STT-RAM
Worst case tso (ns)	4.070	10.010
Worst case tcu (ns)	12.408	6.809
Worst case th (ns)	1.730	-1.517
Clock period (ns)	4.195	3.609

The comparison of time constraint is tabulated in Table 2. The worst case of STT-RAM is very twice that of SRAM. Eventhough worst case tso is more for STT-RAM worst case tcu and worst case th is very much less than SRAM. So only we choose STT-RAM over SRAM. The clock period of both will also differ in a very slight number which indicates that read and write operation always needs same clock pulse rate. Frequency can be also calculated which is inverse of clock rate in seconds unit.

CONCLUSION

We now proposed a novel method where Z-TCAM is implemented with STT-RAM which replaces SRAM. STT-RAM is a latest type of non-volatile memory and has main applications in present on technology and data-center power application. Its MTJ and layer architecture provides much more intensive read/write operation. Our technique provides a much more accurate description of the MTJ resistance switching during the write operation of an STT-RAM cell. An STT-RAM main memory can achieve high performance compared to all other main memory and it brings 60% reduction in average memory subsystem energy. Subsequently, the range, delay and force are lessened by utilizing STT-RAM. It has almost unlimited endurance. Moreover, the proposed ZTCAM is having a simple structure and importantly, have deterministic search performance of one word comparison per clock cycle.

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