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Performance Analysis of Electronic Ballast in CFL Application Using Sepic and CUK Converter Topology

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Abstract: This syudy is based on the reduction of power quality issues, using converter topology for Compact Fluorescent Lamp (CFL) applications. While concentrating on the parameters such as Total Harmonic Distortion (THD), Power factor and output voltage DC-DC converter topology is compared. On the performance analysis of Single-Ended Primary-Inductor Converter (SEPIC) and CUK converter, all the above parameters for the various duty ratio are analyzed and measured. To obtain steady state output voltage of both the converter are made to be operated in the closed loop system using PI Controller. In order to reduce the switching losses and achieving the Zero Voltage Switching (ZVS) the switching frequency of the Series Resonant Parallel Loaded Inverter (SRPLI) made to be greater than the resonant frequency. To analyze the above parameter for the various duty cycle value of the above converter topology are designed by using MATLAB/Simulink Model. The observed values of THD, power factor and output voltage are tabulated and compared.

Key words: CUK converter, SEPIC converter, THD, power factor, topology

INTRODUCTION

In a popular growth of the lighting industry, CFL lamp recorded a better growth based on the weight, size, low cost, luminous efficiency and power consumption. In the CFL lamp due to the production of negative characteristics in an operating region the ignition process will be affected. To avoid the sudden rise of voltage and to perform the lamp in a steady state process the ballast is introduced. The ballast circuit consists of an EMI filter, bridge rectifier, DC-DC converter and an inverter.

For the power factor correction stage DC-DC converter is analyzed for providing an amplifier output voltage. The power factor is to be improved at two stages. They are the high power factor regulator stage which converts AC main voltage into DC voltage and conversion of DC voltage into a high frequency AC voltage to drive the lamp. In the power conversion process the harmonics are produced in the circuit and results the distorted current waveform. An EMI filter is designed to eliminate the harmonic components generated in the lamp circuit Fig. 1. The various components in the ballast circuit are shown in Fig.1. An implementation of two integrated Flyback Converter in the circuit need a high voltage for controlling the switching operation. Due to the coupling of the inductances the flickering of current is observed (Calleja *et al*., 1999). While using Buck Boost Converter in a fluorescent lamp, the magnitude of output voltage is reduced and also it needs to control loops for sustaining the input current and output voltage (Shrivastava and Singh, 2010). It is also suggested that crest factor is also included in the power quality problems, it should be ≤1.7.

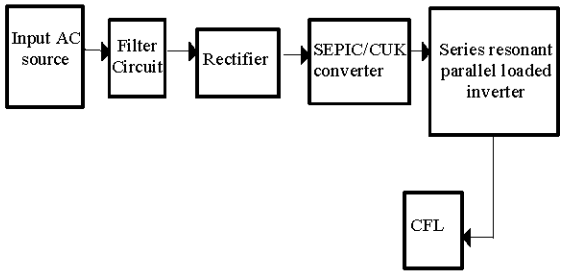

Fig. 1: Block diagram for ballast circuit of CFL lamp

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MATERIALS AND METHODS

Sepic converter: The schematic diagram for an electronic ballast circuit is shown in Fig. 2 which consists of a SEPIC Converter to drive the CFL lamp. By operating SEPIC Converter in the discontinuous mode of operation the stable output voltage is striking for the lamp's ignition process (Simonetti *et al*., 1997).

The SEPIC Converter has an advantage of low voltage stress and it also does not have the reverse polarity as in the Buck Boost converter. During pre-heating stage the lamp voltage is decreased which results the increasing of DC current to preheat the cathode filament. Now the power of the lamp has to be maintained in an average condition (Lam *et al*., 2008). By using the single switch converter (Lam and Jain, 2010), lamp power can be controlled. For further reduction of the voltage stress, the MOSFET switching device with a PI controller to be used (Fraytag *et al*., 2015; Silva *et al*., 2013).

During the ignition stage, the DC link voltage has increased linearly and can be limited to a nominal value. In starting condition the input current decreases simultaneously with DC link voltage and provides constant lamp power for improving brightness (Hu *et al*., 2012). When S is turned on during the steady state condition, the input voltage V_{in} and passes through the inductor L_1, stores magnetic energy. Then the current in the inductor L_2 charge the capacitor C_2 which dissipates the energy to the load R. The design components for SEPIC converter. In a discontinuous mode of operation the duty cycle (D) can be defined as:

$$D=\frac{v_0}{v_{in}+v_0} \tag{1}$$

Based on the ripple current the inductance value of L_1 is selected and the current of the inductor should be at 20% of peak current:

$$L_x=\frac{V_{in}D}{2\Delta I_L f_s} \tag{2}$$

The selection of capacitor C_1 depends on the output current:

$$C_1=\frac{I_o D}{\Delta V_{c1} f_s} \tag{3}$$

$$C_2=\frac{I_o D}{\Delta V_{RPL1} f_s} \tag{4}$$

Cuk converter: The schematic diagram for an electronic ballast circuit is shown in Fig. 3 which consists of CUK converter to drive the CFL lamp. This converter has operated in a Continuous Conduction Mode (CCM) along with a half bridge resonant inverter for stabilizing the output voltage with constant lamp current. Through CCM operation, the current through the inductor remains constant over the cycle. By using the half bridge resonant inverter the higher order harmonics can be filtered easily.

Design components of cuk converter: For the CCM operation the duty cycle can be defined as:

$$D=\frac{V_o}{V_{in}+V_o} \tag{5}$$

The value of inductance L1 and L2 should be 20% of output current. Hence, it is expressed as:

$$L_1=\frac{V_{in}.D}{\Delta I_L.f_s} \tag{6}$$

The coupling capacitor is estimated based on the ripple current:

$$C_1=\frac{I_o D}{\Delta V_{c1} f_s} \tag{7}$$

The capacitance Co has a capacitance to maintain a DC voltage component and must provide a continuous load current at high switching frequency.

Series Resonant Parallel Loaded Inverter (SRPLI): It contains a half bridge inverter with a filter circuit for blocking DC voltage generated by a converter. In general the transformer windings are used to step up and step down the voltage and to provide steady state value for ignition process. But this windings may affect the lamp life. To overcome this issue,block the DC voltage and provide soft ignition process, a resonant inverter to be used. If the switching frequency is equal to the resonance frequency during the ignition process, a high voltage generation is produced across the lamp (Garcia *et al*., 2013).

The capacitor C_b is used to block the DC components from the square wave inverter. Otherwise, it distorts the lamp current. The capacitance C_b is should be chosen higher than the parallel resonant capacitance C_p shown in

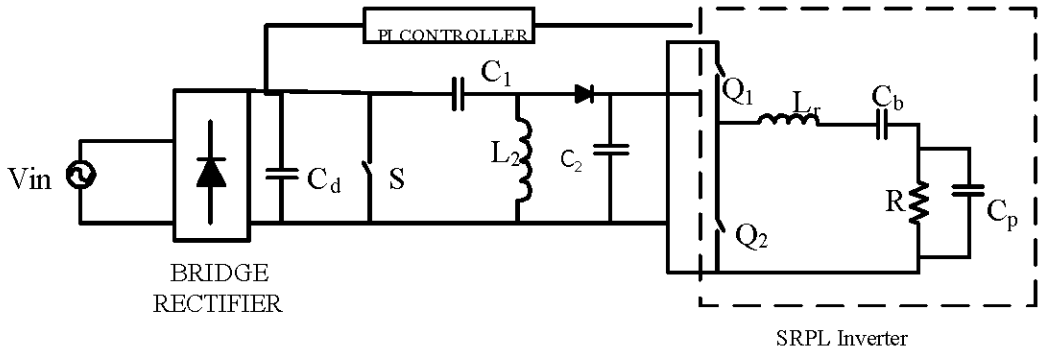

Fig. 2: Circuit diagram for SEPIC converter

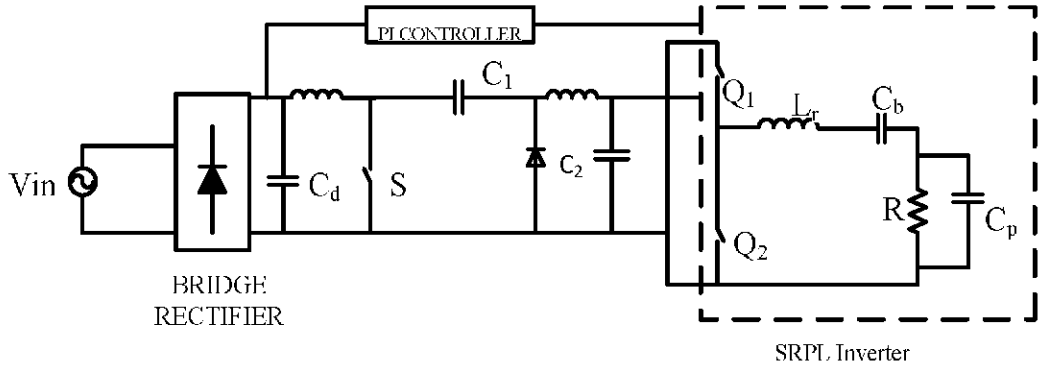

Fig. 3: Circuit diagram for CUK converter

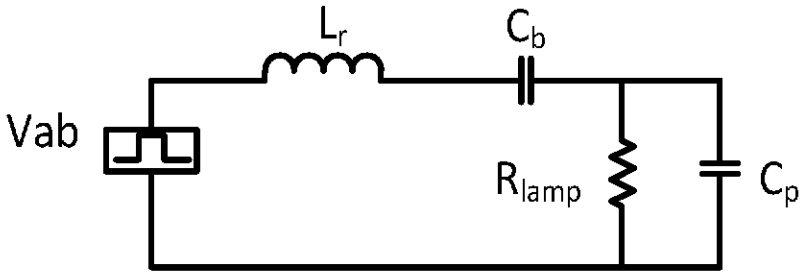

Fig. 4: Circuit diagram for SRPL inverter

Fig. 4. To reduce the switching losses, switching frequency must be greater than the resonant frequency, hence ZVS is achieved.

RESULTS AND DISCUSSION

The operation of the SEPIC Converter with a PI controller using MATLAB simulation is shown in Fig. 5. By using the PI controller the lamp voltage can be maintained constant during the ignition stage and is explained in Table 1 and Fig. 5. The lamp circuit is designed to operate from the source voltage of 220 V. During the preheating stage, the current flow is low and it is gradually increasing in the ignition stage. For the input value of 220 V_{rms} the output voltage of 110 V is obtained. The characteristics of harmonics to be analyzed for the proposed circuit is shown in Fig. 6 and 7. The result of CUK with, PI controller using MATLAB simulation are shown.

CUK converter is designed by using the MATLAB circuit shown in Fig. 8 and 9. For the input voltage of 220 V_{rms} the operation of the converter with closed loop system is shown in the Fig. 10 and 11. The lamp voltage of 150 V is obtained from the duty ratio of 0.5.

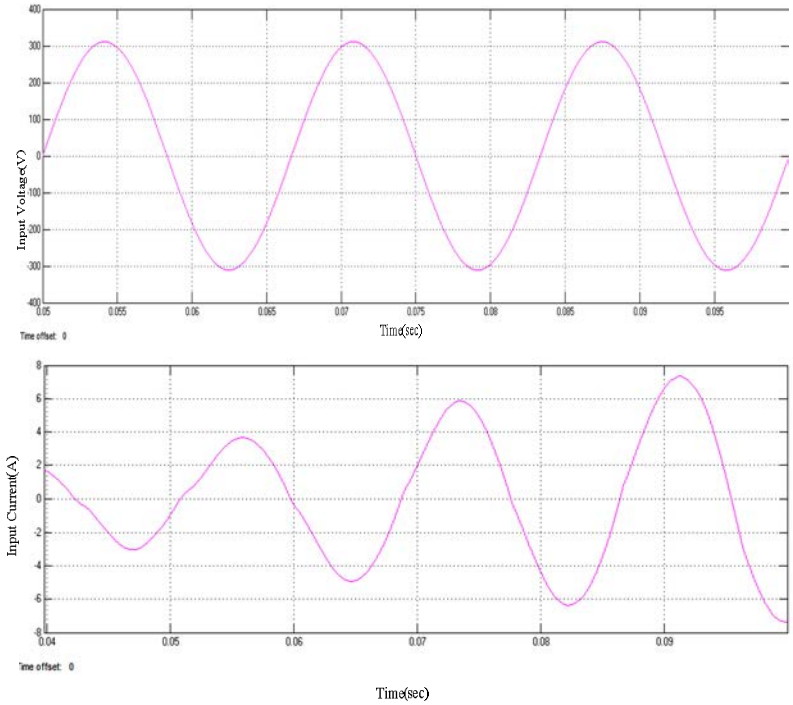

Fig. 5: a) Input voltage waveform for SEPIC converter; b) Input current waveform for SEPIC converter

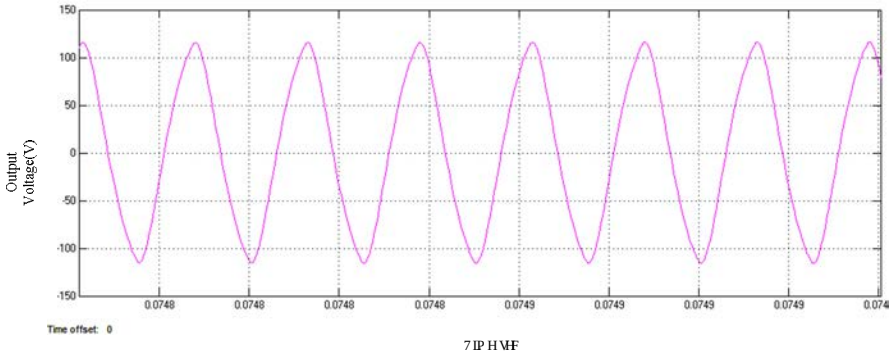

Fig. 6: Waveform for output voltages of the lamp

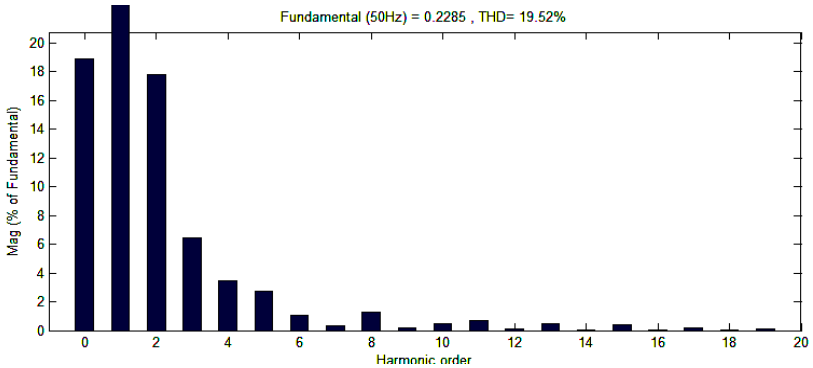

Fig. 7: Harmonic spectrum for lamp current using SEPIC converter

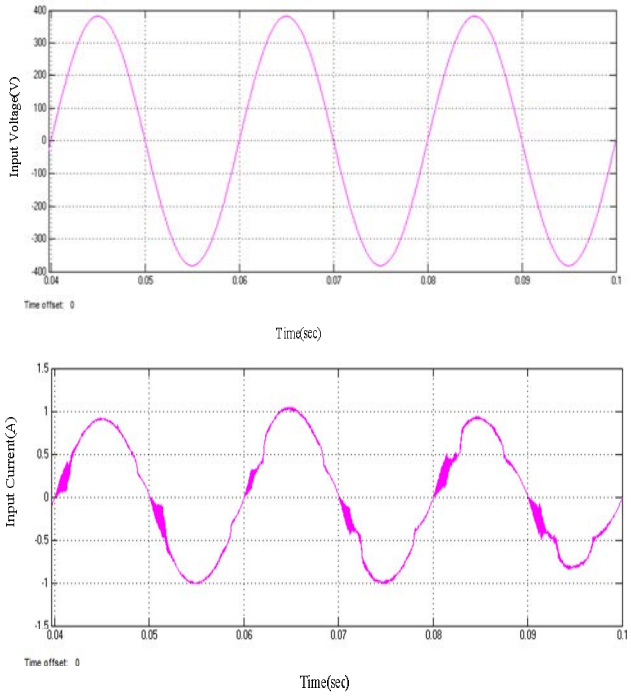

Fig. 8: a) Input voltage waveform for CUK converter; b) Input current waveform for CUK converter

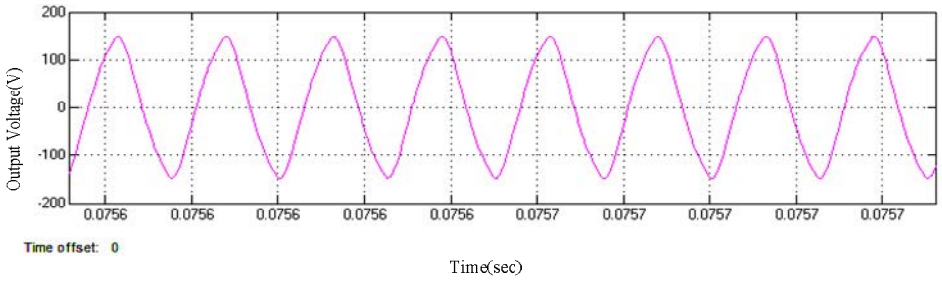

Fig. 9: Waveform for output voltage of lamp using CUK converter

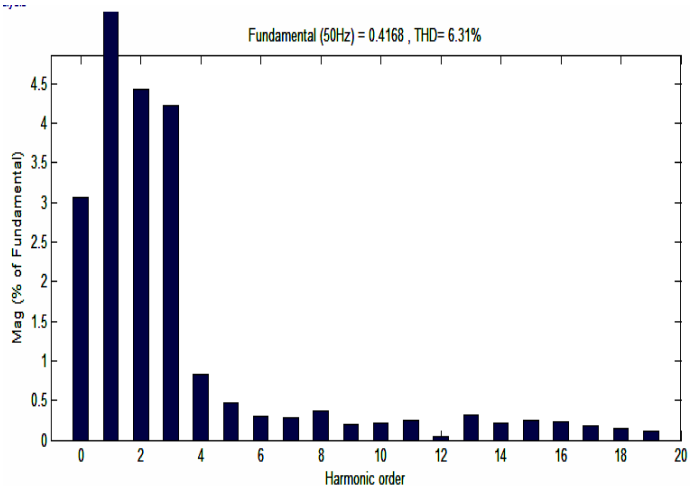

Fig. 10: Harmonic spectrum for lamp current using CUK converter

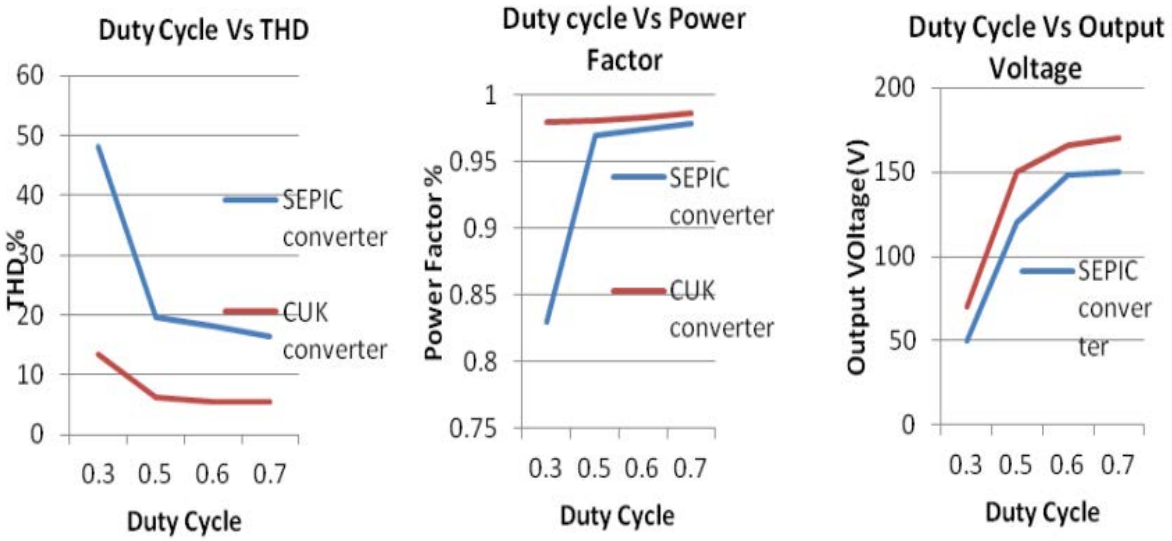

Fig. 11: Analysis of THD, power factor and output voltage of two converters for various duty cycles

Table 1: Comparative analysis of SEPIC converter with CUK Converter analysis of the various duty cycle values

	SEPIC converter			CUK converter		
Duty ratio	Output Voltage (V)	THD (%)	Power factor	Output Voltage (V)	THD (%)	Power factor
0.3	50	48.10	0.830	70	13.45	0.980
0.5	120	19.52	0.970	150	6.300	0.981
0.6	148	18.10	0.974	166	5.590	0.983
0.7	150	16.40	0.979	170	5.500	0.986

On the basis of above results the SEPIC Converter produces an output voltage of 120 V with higher THD level. But in CUK converter the harmonic's level to be low, even for high output voltage. Also the CUK Converter maintains longer lamp life than the SEPIC Converter.But based on the cost, CUK converter is little high (Table 1).

CONCLUSION

From the proposed analysis of both the Converter results, we conclude that in the various duty cycles, the CUK Converter is able to operate with good power factor (0.98), lower in harmonic distortion (6.3% THD) and more output voltage (150 V) for the duty ratio of 0.5. Similarly for the various duty cycle values we have seen that the performance of CUK Converter is better than SEPIC Converter. By using the PI Controller the converter voltage gets amplified and ZVS is achieved by using SRPLI stage. Also, this analysis shows that the CUK Converter provides more stable operation and more output voltage than the SEPIC Converter for the same duty ratio of 0.5.

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