# Comparative Analysis of Low Power Full Adders and 4×4 Vedic Multipliers

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**Abstract:** The design of low power multipliers is the basic necessity for the design and the implementation of efficient power aware devices. Multipliers play a major role in digital signal processing applications. In multiplication, reliability is strongly affected by power consumption. Here Vedic multiplier is designed by the principles of Vedic Mathematics which is the ancient Indian system of mathematics. In this study four 4×4 Vedic multipliers are designed based on four different logic full adders such as 28T, TGFA, 14T and 16T. These multipliers and full adders were designed and simulated using microwind 2 electronic design automation tool with 0.12 μm technology. Finally a comparison is made on the performance of full adders and Vedic multipliers based on power consumption and transistor count.

**Key words:** Full adder, Vedic multiplier, power consumption, digital signal processor, CMOS

## INTRODUCTION

As the range of integration keeps growing, more and more sophisticated signal processing systems are being implemented on a VLSI chip. Most of the signal processing applications not only demand great computation capacity but also consume considerable amount of energy. Hence, power consumption has become a critical aspect in today's VLSI system design. The need for low-power circuits arises from two main factors: First, due to high operating frequency and processing capacity per chip, delivering of large currents, heat emitted due to large power consumption and the need for proper cooling techniques. Second, due to the limited battery life in portable electronic devices. Low power design directly leads to prolonged operation time in these portable devices. Multiplication is the basic operation in ALU unit most signal processing algorithms. Multipliers have long latency, large area and consume more power. Therefore, design of low power multipliers play an important role in low power VLSI system design (Sze, 1988).

Multiplier functions as an important element of the digital signal processor and in various other applications. The performance of the digital signal processor can be improved only based on the performance of the multiplier. With advances in technology researchers are trying to design multipliers which offer either of the following design targets; low power consumption, high speed, regularity of layout, small area and even combination of these in one multiplier. A multiplier is one of the key hardware blocks in most Digital Signal Processing

(DSP) systems. Multiplier plays an important role in digital filtering, digital communications and spectral analysis.

Many DSP applications are targeted at portable battery operated systems so the power dissipation becomes one of the essential primary design constraints. Since multipliers are complex circuits and must typically operate at a high system clock rate, so reducing the delay of a multiplier is a crucial part of satisfying the overall design (Garg and Rai 2012). Moreover, application specific integrated circuits rely on efficient implementation of the arithmetic circuits required in the execution of the algorithms. Also, the increase in the number of transistor results in the increase in the complexity of the arithmetic circuits thus leading to more power consumption.

Consequently, the design of low power multipliers is a basic necessity for the design and implementation of efficient power aware devices. This serves as a motivation in the design of low power VLSI circuits. But, reducing the power consumption and enhancing the circuit design pose challenges in the multiplication and accumulation. Hence, the need for research on dynamic power reduction and static power reduction in the design of circuits become evident. Researchers have recognized the importance of designing low power multipliers. Some research has resulted in low power circuit designs for multipliers. This research has focused on designing low power multipliers using four such circuit designs.

## MATERIALS AND METHODS

**Vedic multiplier:** Vedic Mathematics (VM) is the name given to the ancient Indian system of mathematics that

was rediscovered in early 20th century. VM is mainly based on 16 principles or word formulae which are termed as Sutras (Kumar and Charishma 2012). A simple Vedic multiplier architecture based on the Urdhva Triyagbhyam (Vertically and Cross wise) Sutra is presented. This Sutra was traditionally used in ancient period of India for the multiplication of two decimal numbers in relatively less time. The hardware of the Vedic multiplier is shown to be very much similar to that of the array multiplier. It is also equally likely that many such applications might come up from the storehouse of knowledge Veda, if investigated properly.

VM is part of four Vedas (books of wisdom). It is part of Sthapatya-Veda (concepts of Civil Engineering and Architecture) which is an upa-veda of Atharva Veda. It covers explanation of several modern mathematical terms including arithmetic, geometry trigonometry, quadratic equations, factorization and even calculus. After extensive research in Atharva Veda, 16 sutras (formulae) and 16 Upa sutras (sub formulae) were constructed. The very word 'Veda' has the derivational meaning of fountain head and illimitable storehouse of all knowledge. VM is the name given to the ancient system of mathematics which has unique technique of calculations based on simple rules and principles with which many mathematical problems can be solved (Poornima *et al.*, 2013).

The system is based on 16 Vedic sutras or aphorisms, which are actually word formulae describing simple natural ways of solving a whole range of mathematical problems. The beauty of VM lies in the fact that it reduces the otherwise cumbersome looking calculations in existing mathematics to a very simple one. This is so because the Vedic formulae based on the principles of human mind works. This is a very interesting area and presents some effective algorithms which can be applied to various fields of engineering such as computing and digital signal processing.

Multiplication methods are extensively discussed in Vedic Mathematics. Various interesting tricks and short cuts are suggested by VM to optimize the process. These methods are based on concept of one multiplication using deficits and excess two changing the base to simplify the operation. Various methods of multiplication proposed in VM are:

- Urdhva Tiryagbhyam-vertically and crosswise
- Nikhilam Navatashcharamam Dashatah: All from nine and last from ten
- Anurupyena: Proportionately Vinculum

The hardware architecture of 2×2 and 4×4 bit Vedic multiplier module are displayed. Here, Urdhva Tiryagbhyam (vertically and crosswise) sutra is used to propose such architecture for the multiplication of two
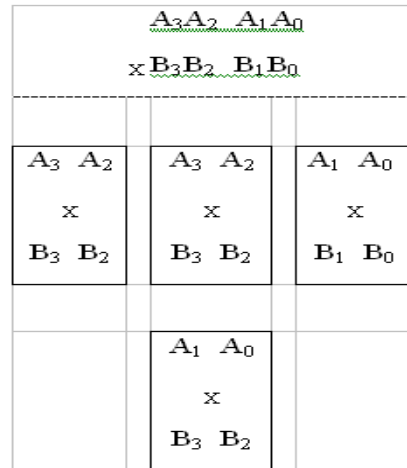


Fig. 1: 4×4 Vedic multiplier

binary numbers. The beauty of Vedic multiplier is that here partial product generation and additions are done concurrently. Hence, it is well adapted to parallel processing. The feature makes it more attractive for binary multiplications. This in turn reduces power which is the primary motivation behind this work.

The 4×4 bit Vedic multiplier module shown in Fig. 1 is implemented using four 2×2 bit Vedic multiplier modules. The inputs of the module are A= A3 A2 A1 A0, B = B3 B2 B1 B0 and output is S7 S6 S5 S4 S3 S2 S1 S0. Here A and B are divided into two parts that is A3A2 and A1 A0 for A and B3 B2 and B1B0 for B.

Each block as shown is 2×2 bit Vedic multiplier. First 2×2 bit multiplier inputs are A1A0 and B1B0. The last block is 2×2 bit multiplier with inputs A3 A2 and B3 B2. The middle one shows two 2×2 bit multiplier with inputs A3 A2 and B1B0 and A1A0 and B3 B2. So, the final result of multiplication, which is of 8 bit, S7 S6 S5 S4 S3 S2 S1 S0. To get final product (S7 S6 S5 S4 S3 S2 S1 S0), four 2×2 bit Vedic multiplier and three 4-bit Ripple-Carry (RC) Adders are required (Anju Agarwal 2013). This Vedic multiplier can be used to reduce delay. Early literature speaks about Vedic multipliers based on array multiplier structures. But, this architecture is efficient in terms of speed and parallel processing. Interestingly, 8×8 Vedic multiplier modules are implemented easily by using four 4×4 multiplier modules.

## RESULTS AND DISCUSSION

**Design of vedic multipliers using various logic full adders**
**Vedic multiplier based on 28T full adder:** Adders form to be the an important component in the applications such
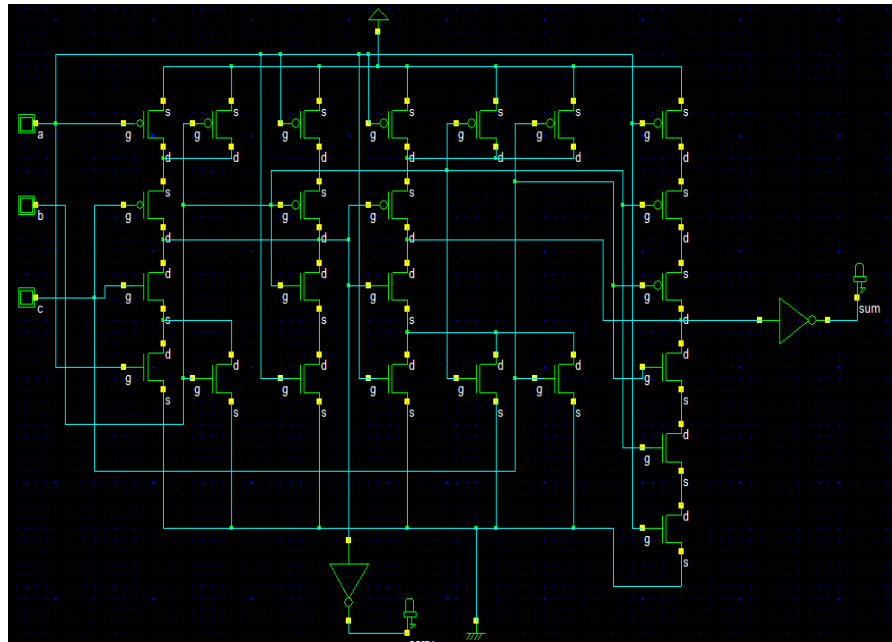
Fig. 2: The 28T Full adder

as digital signal processing and microprocessors architectures. The importance of the digital computing lies in the full adder design (Naveen *et al.*, 2014). Conventional three bit full adder consists of 28 transistors and is shown in Fig. 2. CMOS implementation consists of two functional blocks, pull-up and pull-down. Pull-up block is implemented with P-channel MOS transistors and pull-down block is implemented with N-channel MOS transistors. The most essential advantages of this full adder was its high noise margins and thus reliable operation at low voltages (Damle *et al.*, 2013). The layout of CMOS gates was also simplified due to the complementary transistor pairs. The high noise margin and voltage scaling design makes them highly advantageous over others. Due to complementary relationship between pull-up and pull-down functional block, the combination of which turns OFF the pull-up transistor will turn ON the pull down block and vice-versa. This eliminates the possibility of occurring floating output. Pull down functional block is constructed using nMOS devices whereas, pMOS devices are used for pull up functional block. The main reason for this choice is that nMOSFET transistors produce strong '0' and pMOSFET transistors give strong '1'. A pMOS switch is able to charge the output to vdd and nMOS fails to raise the output above (vdd to vtn). In CMOS logic, all switches in pull-up block are implemented by using pMOS transistors whereas in pull-down network, all switches are implemented by using nMOS transistors. A 4×4 Vedic multiplier is designed based on this 28 T full adder and it

is shown in Fig. 3.The design has four 2*2 Vedic multipliers, three ripple carry adders and addition is performed by using 28T full adder.

**Vedic multiplier based on TGFA:** A CMOS transmission gate shown in Fig. 4 is created by connecting an nFET and pFET in parallel. The nFETMn is controlled by the signals while the pFETMp is controlled by the complement. When wired in this manner, the pair acts as a electrical switch between the input variable x and the output variable y, respectively. The operation mode of the switch can be easily understood by analyzing the two cases for s. If s = 0, the nFET transistor is OFF; since s = 1, the pFET transistor is also OFF, so that the Transmission gate acts as an open switch.The transmission gate based full adder produces outputs of correct polarity for both sum and carry with the disadvantage of high power consumption. The circuit has two inverters followed by two transmission gates which act as 8T-XOR (Chede *et al.*, 2010). It is the fastest adder and is also simpler compared to conventional adder.

The 4×4 Vedic multiplier with Transmission Gate Full Adder as shown in Fig. 5 has less transistor count when compared to the conventional adder. It also consumes less power when compared to the conventional full adder. An important electrical feature of the transmission gate is that there are no direct signal connections to the power supply or ground. Transmission gate appears to be an RC
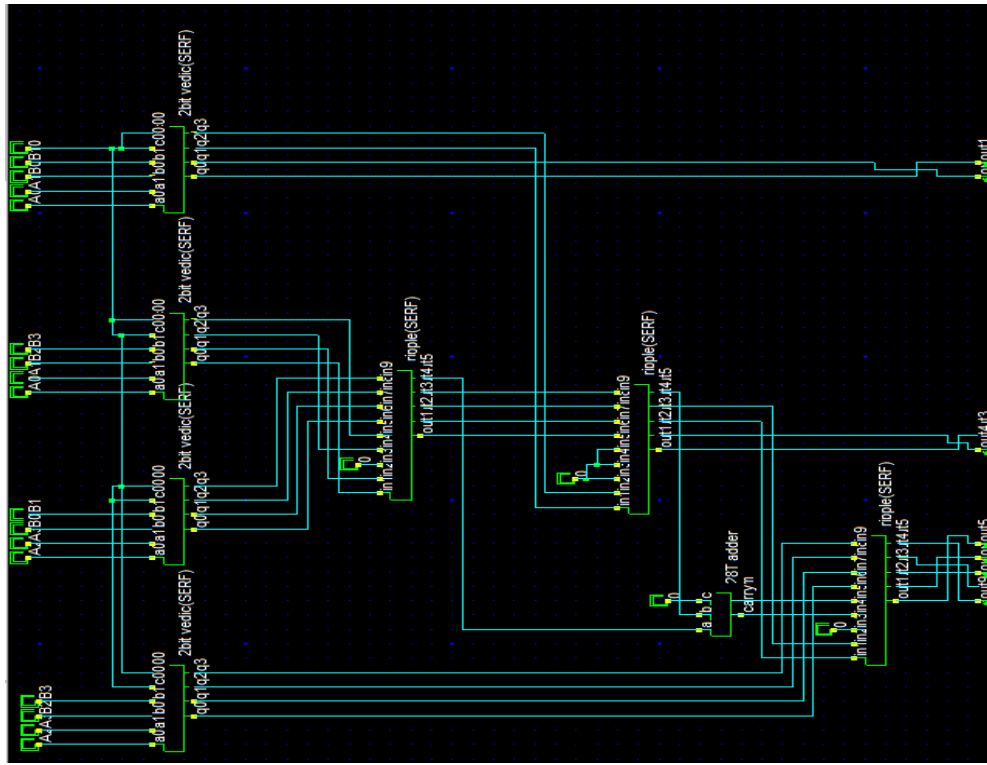
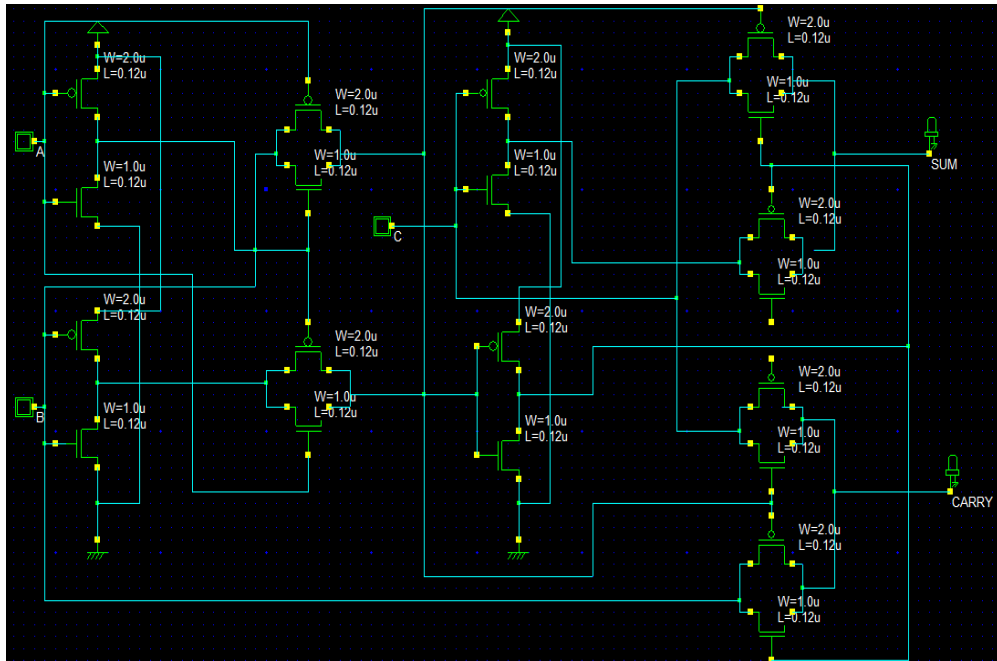Fig. 3: Vedic multiplier based on 28T full adder



Fig. 4: TGFA

parasitic to the driving gate so the response is slower than if the transmission gate were absent. Additional buffer circuits are thus needed to maintain the speed.

**Vedic multiplier based on 14T full adder:** The improved 14T adder cell requires only 14 transistors to realize the adder function and is shown in Fig. 6 (Vigneswaran *et al.*
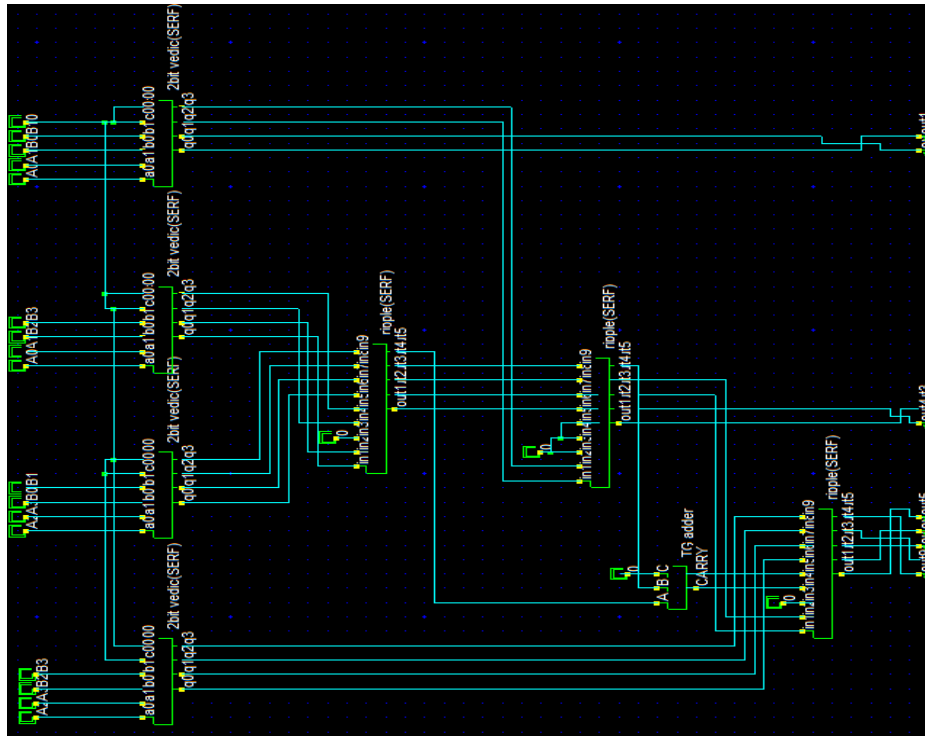
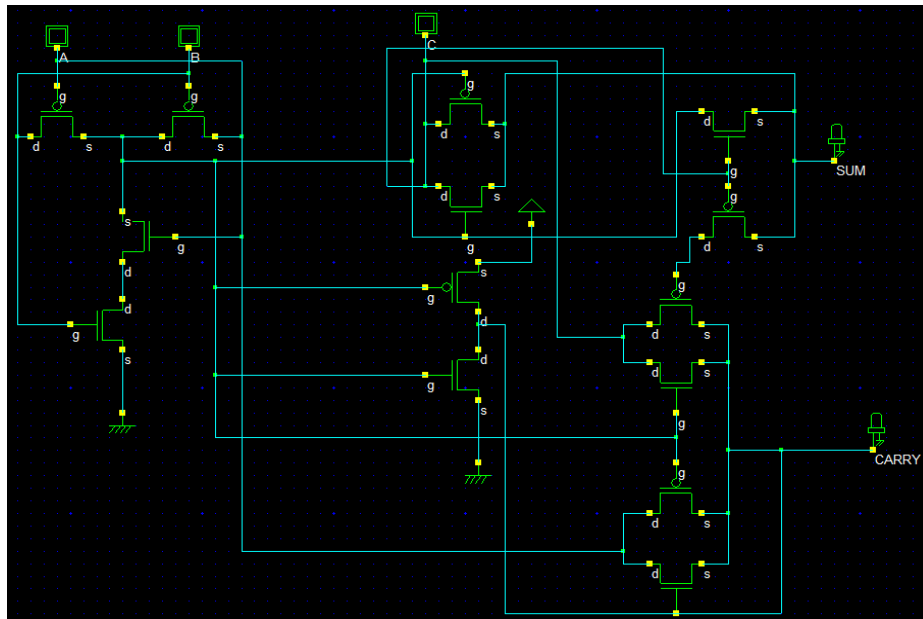Fig. 5: Vedic multiplier based on TGFA



Fig. 6: The 14T Full adder

2006). It produces better result in threshold loss, speed and power by sacrificing four extra transistors per adder cell. Even though, the number of transistor increases by four per adder cell, it reduces the threshold loss problem, which exists in the previous discussed adders by inserting the inverter between XOR Gate outputs to form XNOR gate. The 14T full adder contains a 4T pass transistor logic XOR gate, an inverter and two transmission gates based multiplexer designs for sum and carry signals. This circuit has only 4 transistors XOR
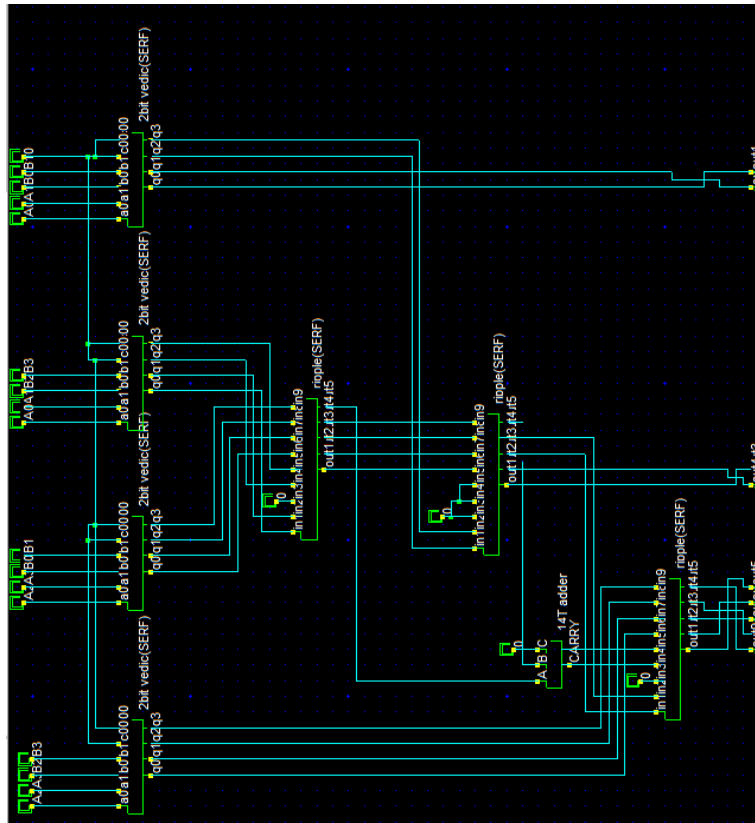
Fig. 7: Vedic multiplier based on 14T full adder

function which in the next stage is inverted to produce XNOR function. These XOR and XNOR functions are used simultaneously to generate sum and carry. The signals C and Cbar are multiplexed which can be controlled either by A XNOR B or A XOR B. Similarly the carry can be generated by multiplexing A and C controlled by A XOR B. The significant advantage of this 14T adder is that it is the fastest and simpler than conventional full adder. The major disadvantage of this full adder is the power dissipation which is large when compared with the conventional adder. However, with same power consumption it performs faster. The Vedic multiplier with 14T full adder as shown in Fig. 7 is one of the area efficient multiplier design when compared with the conventional adder and transmission gate adder. The 14T adder consists of 14 transistors. The circuit has two inverters followed by two transmission gates which act as 8T-XOR.

**Vedic multiplier based on 16T full adder:** CMOS employs both n-type and p-type transistors to realize logic functions. Today, CMOS technology has carved a niche for itself as the feasible semiconductor VLSI technology for microprocessor, memories and ASICs.

A 16T adder is shown in Fig. 8. It is an improved version from 14T. It is the same as 14T in terms of the output modules. However, the XOR-XNOR functional module has been modified to reduce power consumption and delay.

The 4×4 Vedic multiplier with 16T Full adder as shown in Fig. 9 has XOR-XNOR modules does not have full-swing outputs thus, the transistors which have been connected to this functional module are turned ON or OFF slowly.

The circuit operates with full swing voltage output but consumes significant power and has more delay compared to adders having less transistor count. It uses the low-power designs of the XOR and XNOR logic gates, transmission gates and pass transistors. Eliminating an inverter and the short circuit power component in addition to reducing cell capacitances would result in low power consumption and delay.

The 4×4 Vedic multiplier was design using 28T, TGFA, 14T and 16T Full adder logics. Initially these adders were designed, simulated and a comparison is made on the performance of these four adders based on transistor count and power consumption as depicted in
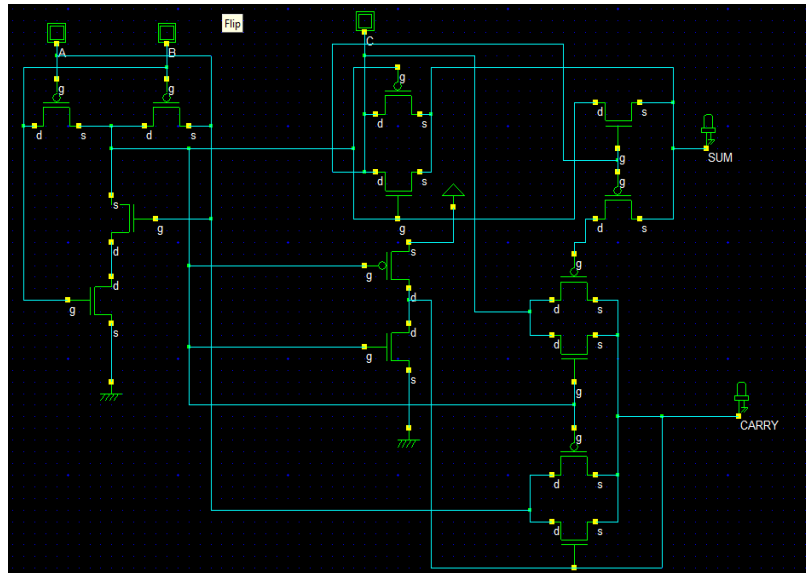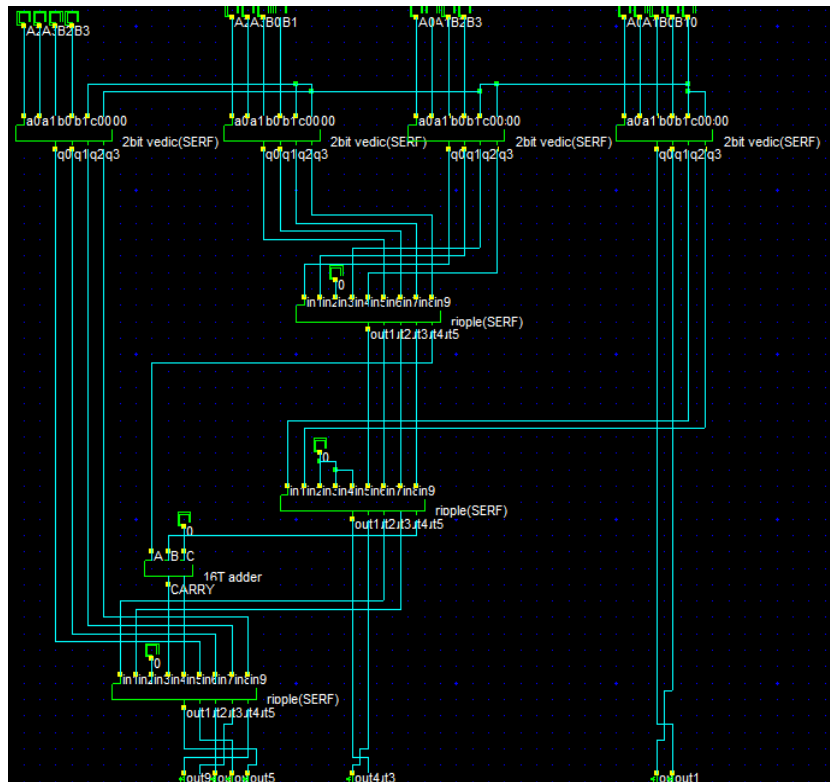
Fig. 8: The 16T Full adder



Fig. 9: Vedic multiplier based on 16T full adder

Table 1: Comparison on the performance of adders

| Adder | Transistor count | Power consumption (nW) |
|---|---|---|
| Conventional adder | 28 | 91.66 |
| TG adder | 20 | 51.82 |
| 14T adder | 14 | 207.4 |
| 16T adder | 16 | 85.04 |

Table 1. The 4 Vedic multipliers based on above mentioned adders were designed using DSCH2 tool and the results were simulated using 0.12µm technology in Microwind 2 Tool. Finally, a comparison of the performance of the Vedic

Table 2: Comparison on the performance of vedic multipliers

| Vedic Multiplier | Transistor count | Power consumption (mW) |
|---|---|---|
| 28T Full adder | 588 | 0.723 |
| TGFA | 420 | 0.671 |
| 14T Full adder | 294 | 0.587 |
| 16T Full adder | 336 | 0.510 |

multipliers is made based on the transistor count and power consumption which is tabulated in Table 2.

## CONCLUSION

Digital multipliers are the core components of high performance systems, whose performances are generally determined by the performance of the multiplier. Multiplier is the main key structure for designing an energy efficient processor and a multiplier design decides the efficiency of a digital signal processor. Most of the signal processing applications not only demand great computation capacity, but also consume considerable amount of energy. Hence, power consumption has become a critical aspect in today's VLSI system design and the design of low power multipliers plays an important role in low power VLSI system design. The 4×4 Vedic multiplier was designed based on four different full adders namely 28T,TGFA,14T and 16T.The power consumption and transistor count of the these Vedic multipliers were simulated using $0.12\mu$m technology in Microwind 2 Tool. The overall comparison of the performance of the four Vedic multipliers was performed. Based on the comparison, the Vedic multiplier with 14T full adder has less transistor count and Vedic multiplier with 16T full adder has less power consumption.

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