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Development of a One Touch Information Relay System for Distress Calls-Digital Circuit Design

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Abstract: The design of a one touch 16-bit information relay system digital circuit for distress calls is the focus of this research. The digital circuit consist of binary switches which forms the pre-coded digital signal required for serial information transfer with the use of a multiplexer. The circuit was analyzed with the use of Multisim-10 application software to assess its response to coded information.

Key words: Binary switches, multiplexers, multi-vibrator, binary counters, frequency, Nigeria

INTRODUCTION

Binary information stored in a digital system can be classified as either data or control information. Data are discrete elements of information that can be manipulated in the form of arithmetic, logic, shift and other similar data processing tasks. These operations are implemented with digital complements such as adders, registers, decoders, multiplexers and counters (Tocci, 2002; Anokh and Chabra, 2003).

The logic design of a digital system can be divided into two distinct parts. One part is concerned with the design of the digital circuit that permits the data processing operations. The other part is concerned with the design of the control circuit that supervises the operations and their sequence (Batho, 1992). The relationship between the control logic and the data processor in a digital system is shown in Fig. 1. The data processor subsystem manipulates data in the register according to the system requirements. The control logic initiates proper sequence of command to the data processor. The control logic uses status conditional from the data processor to serve as decision variables for determining the sequence of control signal (Gupta, 2003).

The control logic that generates the signals for sequencing the operations in the data processor is a sequential circuit whose internal states dictate the control commands in the system. At any given time, the state of the sequential control initiates a preset set of commands (Gupta, 2003; Batho, 1992). Depending on the status conditions and other external inputs, the sequential control goes to the next state to initiate other operations. The digital circuit that acts as the control logic provides a time sequence of signals for initiating the operations in the data processor and also determines the next state of the control subsystem itself. In this research, a 16-input multiplexer is the data processor with the control logic formed by the counters with its clock generator (Tocci, 2002).

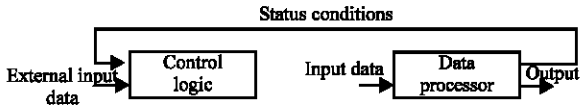

Fig. 1: Control and data processor interaction

MATERIALS AND METHODS

Design of a 16-bit information relay system: This is achieved by using a 16-input Multiplexer (MUX) or data selector for coding purpose as shown in Fig. 2. The 16 binary switches represent the pre-coded data to be transferred to a remote location which consists of two 8-in-line miniature switches J1 and J2 required for the coding of the multiplexer (Sheda, 2004; Tocci, 2002). In order to activate the multiplexer, a counter is required.

This is selected as a 74LS193N. The clock frequency for the counter and the multiplexer was generated through an NE555 timer to give a frequency of 5 kHz using the equation (Anokh and Chabra, 2003; Sheda, 2004):

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2)C} \quad (1)$$

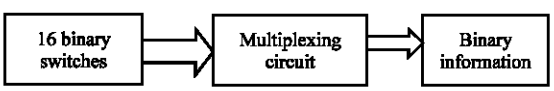

Fig. 2: 16-bit binary information transfer design

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with R_1 = 2.2 kΩ and R_2 = 100 kΩ; the capacitor value C = 1.4 nF and a duty cycle of 50% approx (Gupta, 2003). The ON/OFF switch S1 is designed to be externally accessible to the user while all other components are within the equipment box. The switch S1 is a single-pole-single-throw normally open switch while the other switches for coding are miniature switches. The digital circuit +5V power source and ground are automatically routed in the design. With the switch SI in its off position when there is no distress, it gives a low (0-logic) signal to the input of the 74LS04 inverter (U3D) whose output logic-1 (high state) connects to the input of an OR-gate 74LS32. The output of the OR-gate (U5A) which is in a high state (1-logic), irrespective of the level of the output of U8 and UIB, clears the counter 74LS193N. The output of the inverter also sets the binary counter 74LS293N, through its R_{i1} and R_{i2} pins.

The output of the 74LS193N (U6) counter sets the input of the multiplexer U7-0000 logic which places the output of W at 1 (high-state). The output from the MUX already in the high state is connected to a 74LS08N U4C AND gate whose second input is connected to UIB (74LS08) AND gate being fed by the low-output logic due to the set-signal from SI to 74LS293N (U8) IC to give a low-logic output (0-logic) which turns off the oscillator transmitters switch Q_2, with Q_1 already in the off-state by a signal transmitted by the output of 74LS04 (U3B) inverter fed from the output of the MUX.

For a distress call to be made, the DPOC switches ON SI to place a high (1) logic at the input of the inverter U6D whose output places a low (0) logic signal in one of the inputs of the OR-gate 74LS32N U5A. Already the 2nd input of the U5A gate is at 0-logic from the output of AND gate U4C which gives a low (0) logic at the output of the OR-gate U5A to make the Clear (CLR) input of the synchronous counter U6 inactive. This allows in the incoming frequency from a clock generator with the LOAD pin of the synchronous counter made inactive (1-logic). The multi-vibrator generates a square wave output at its pin 3 which is connected to the counter U6 (UP) counting mode to count from 0000-1111.

The 5V power supply from the battery is connected to switch S1 to supply the required power to the circuit. The counter LS293N U8 IC is connected to the ON/OFF switch through the inverter U3D and the output from the UIB gate regulates the performance and sequence of transfer of the serial information, through its connection to G input of the MUX U7 (Milman and Halkia, 1991). The binary counter U8 determines the number of times it is required to send the coded information through the transmission medium before being turned off (Hudson and Luecke, 1999). In this research, we decided to transmit the signals three times by the connection of Q_B and Q_C output of binary counter U8 to the input of AND gate U4C. The response of the counter U6 to the clock signal by the generator U1 is possible by the switching of the switch S1 to its ON position which makes the clear input of the counter CLR inactive by the signals sent by U5A OR-gate.

The counting sequence of the counter U6 clocks the multiplexer U7 to allow the coded signals set by 16 switches J1-J16 to be passed serially through its output W. The output of the MUX U7 is active low (0-logic), thus the need for an inverter U3B to invert the output of U7 which forms the coded information signal required to be sent to a remote station for further processing (Hudson and Luecke, 1999). In order to control the passage of the coded information, the counter U6 carry output CO is connected to the input INA of LS293N binary counter U8, whose reset pins R_{01} and R_{02} are connected to the ON/OFF switch S1 via the inverter U6D. As the counter U8, counts on every high-low transition of the CO of U6 output, the Q_A-Q_D outputs changes state from 0000-1111.

RESULTS AND DISCUSSION

The one touch information relay system digital circuit results: The coded information formed by the activation of the 16 input switches of Fig. 3 becomes the parallel input signal to the Multiplexer (MUX) U7. The measured digital output voltage of the connecting switches by a multi-meter is either at a voltage of 5v level for generating a 1-logic signal or 0v level for 0-logic. This shows that none of the switching input voltage lies in the indeterminable region.

When the ON/OFF switch S1 (the only accessible input to the user) is activated in Fig. 3, the output from the Multiplexer (MUX) U7 is a serial digital output signal with the high level (1-logic) at 5V and the low level (0-logic) at OV as shown in Fig. 4b with the oscilloscope XSC1. This shows that the coded input digital signal set by the switches forms a parallel input with a serial output from MUX U7. The input digital signal changes state in response to the clock signal transition of Fig. 4a.

The frequency generator formed by NE555 U1 in Fig. 3 shows an output frequency of 5 kHz square wave as measured by oscilloscope XSC1 of Fig. 4a. This frequency clocks the synchronous counter U6 whose output Q_A-Q_D gives a digital count from 0-15 and back. This sequence of counting allows the coded signals set by the 16 switches J1-J16 to pass serially through the MUX output W as shown in Fig. 4b. The frequency generator formed by U1 with its response in Fig. 4a controls the rate at which the parallel digital signal input is transferred

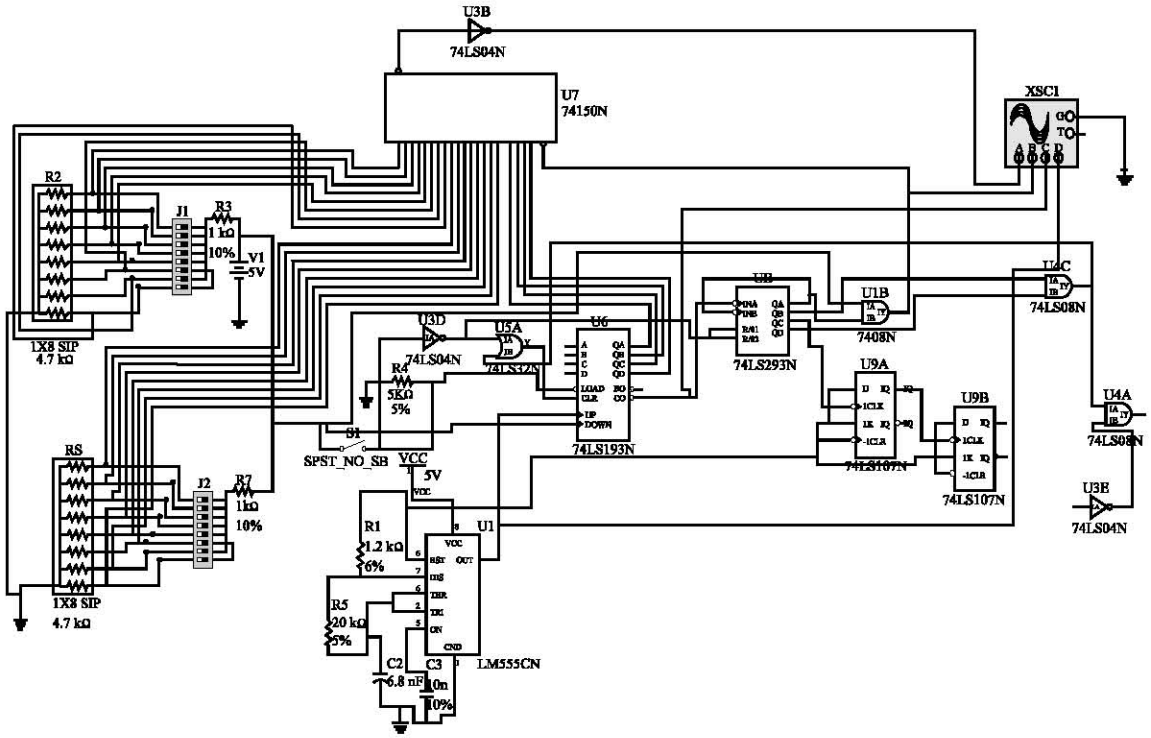

Fig. 3: Digital circuit design for a 16 bit input one touch sender

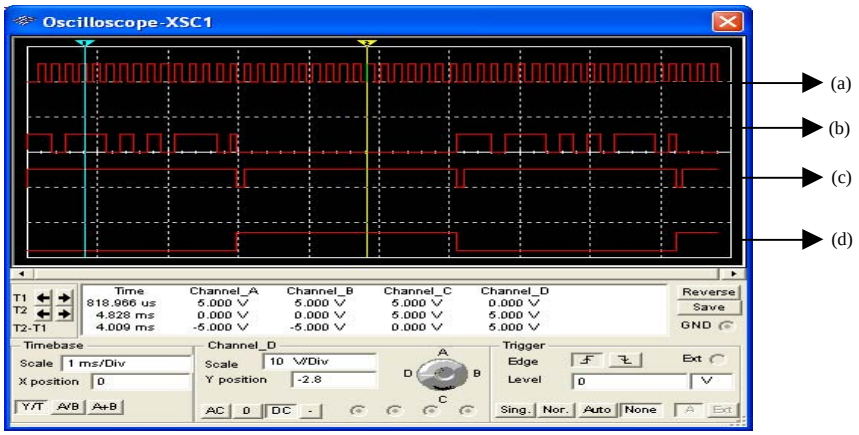

Fig. 4: (a) Frequency generator output response at 5 kHz, (b) Multiplexer (MUX) U7 serial digital output, (c) Counter U6 (CO) carry output and (d) Q_A output of counter U8

through the counting sequence of the synchronous counter U6. The carry output (CO) of the synchronous counter U6 is very important in that it controls the enable/ disable function of the multiplexer U7 response, through the AND gate U1B which is converted to a switching device for signal control of the transfer of the input digital signal from the switches.

The transfer of the coded information is controlled by the synchronous counter U6 carry output (CO) as shown in Fig. 4c which clocks the binary counter U8. The Q_A output of counter U8 changes state as in Fig. 4d at the transition of 1-0 of CO output of U6 of Fig. 4c. The output of AND gate U1B is controlled by the output from the input signal from the counter U8 of Fig. 4d as shown in Fig. 5c. The output of the UIB AND gate is used to clock the G input of the MUX U7 which is active low with its response as shown in Fig. 5d. Thus, UIB AND gate is converted to a switching device for signal control of the

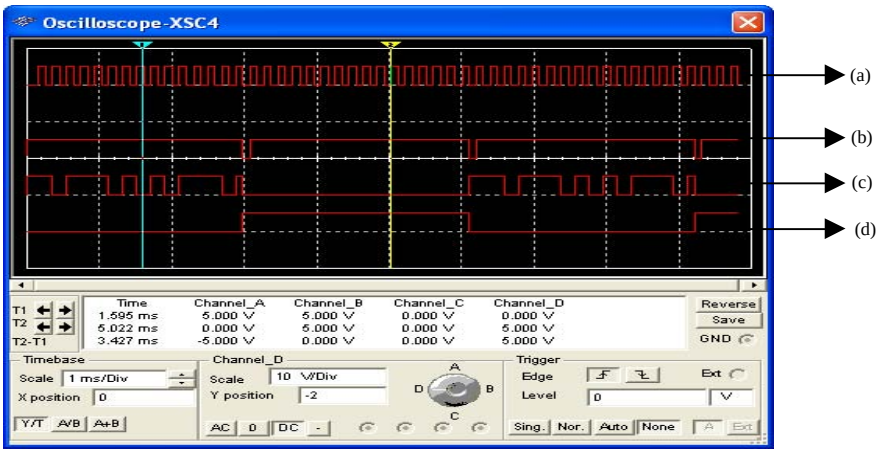

Fig. 5: (a) Clock input, (b) U6 (CO) carry output, (c) AND gate U1B response and (d) G inputs of MUX U7

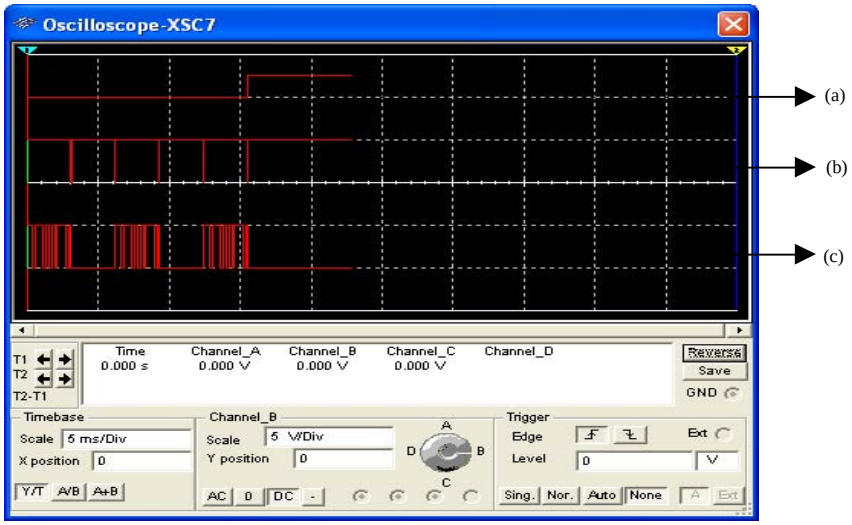

Fig. 6: Control of number of times of transmission of signal response diagram. (a) U4C Output signal, (b) Control signal using CO output of U6 and (c) Signal transmitted (3 times)

transfer of the input digital signal from the switches. Because the second input of UIB AND gate is permanently high, the output is dependent on the output of U6 thus when the output of the UIB AND gate is low, the G input of the MUX U7 is enabled for signal transfer. The disabled G input of MUX U7, disables the MUX output from responding to the clock inputs as shown in Fig. 5d.

Also, the output of counter U8 connects to AND gate U4C to control the switching of the synchronous counter U6 through the Clear (CLR) input and the alarm. From Fig. 5, it can be seen that after 16 clock pulses and the counter CO transition from 1-0 logic, the MUX U7 stops for a count of 16 clock pulses, before another transmission of signal is activated. The number of times the coding signal is allowed to be transmitted is controlled and dependent by which of the outputs of the U8 are connected to the AND gate U4C. For transmission of signal three times for redundancy check of errors at the receiving end the output Q_b and Q_c are connected to U8 inputs and the output results are as shown in Fig. 6. For 4 times, only Q_d of U8 is connected. This shows that with the switch S1 still in the ON position after 3 trials as shown in Fig. 6c, the system is disabled.

CONCLUSION

The development shows that the 16-bit information relay design for distress calls to remote stations. The distress points is pre-coded with the 16-bit binary

information which is interpreted at the remote locations for detailed exact location of call. This can be applied in the design of a localized area security network system.

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